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INAUGURAL SPECIAL ISSUE ON THE DEVELOPING TRENDS OF POWER ELECTRONICS: PART 5

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Editorial for the Inaugural Special Issue on the Developing Trends of Power Electronics: Part 5

WITH this editorial, we sincerely welcome our readers to the brand-new publication — CPSS Transactions on Power Electronics and Applications (CPSS TPEA). It is sponsored and published by China Power Supply Society (CPSS) and technically co-sponsored by IEEE Power Electronics Society (IEEE PELS).

CPSS was founded in 1983 and has been the only top-level national academic society in China that solely focuses on the power supply/power electronics area. In the past 30-plus years CPSS has dedicated to provide to its members, researchers, and industry engineers nationwide with high quality services including conferences, technical training, and various publications, and this in deed has helped the society build up its membership rapidly, which now totals up to more than 4000 individual members plus 500 enterprise members. The fast growth of membership in turn compels CPSS to always work out better services for its members, one of which being the open-up of this periodical — a new journal in English language as a publication platform for international academic exchanging. This of course needs to be done through international cooperation, and that's why IEEE PELS is tightly involved, being the premier international academic organization in power electronics area and one of the fastest growing technical societies of the Institute of Electrical and Electronics Engineers (IEEE).

To fulfill the publishing need of the fast-developing power electronics technology worldwide is a more important purpose of launching this new journal. So far there are only 3 or 4 existing journals which are concentrated on power electronics field and have global reputation. For quite a few years people in the international power electronics community have had the feeling that, the existing journals have not even come close to meeting the huge demand of global academic and technology exchanges. E.g., the two existing IEEE power electronics journals, i.e. IEEE Transactions on Power Electronics (IEEE TPEL) and IEEE Journal of Emerging and Selected Topics in Power Electronics (IEEE JESTPE), now publish about 1000 papers a year, which is under a very low paper acceptance rate of around 25%, but still have a back-log of about one year for the newly accepted papers to finally appear in printed form to the public. The addition of this new dedicated journal would be an ideal improvement to fulfill such a tremendous need.

The booming of publishing need really is an indicator of how fast power electronics has been developing in recent years. Innovations have been continuously coming up from component (both active device and passive device), module, circuit, converter, to system level, covering different technical aspects as topology or structure conceiving, modeling and analysis, control and design, and measurement and testing. New issues and corresponding solutions have been continuously presenting as the applications of power electronics prevail horizontally in almost every area and corner of human society, from industry, residence and commerce, to transportations, and penetrate vertically through every stage of electric energy flow from generation, transmission and distribution, to utilization, in either a public power grid or a stand-alone power system. I personally believe that we are entering a world with "more electronic" power systems. The prediction around 30 years ago, that power electronics one day will become one of the major poles supporting the human society, is coming into reality. And I also believe, that power electronics is going to last for long time as an important topic since it is one of the keys to answer a basic question for human society, which is how human can harness energy more effectively and in a manner friendlier to both the user and the environment.

Therefore, I assume that there is probably no better fitting as for CPSS TPEA to publish its first few issues under a special topic about the developing trends of power electronics. We have invited a group of leading experts in different areas of power electronics to write survey/review papers or special papers with review/overview nature to some extent. To publish in a timely and regular style, we organize this inaugural Special Issue into 5 different parts. Part 1, 2, 3 and 4 were published in the December issue last year and previous issues of this year respectively, Part 5, appearing in this December issue, is the last part of the inaugural Special Issue.

In Part 5 we are honored to have 6 invited papers. The first four address four recently hot or emerging application areas of power electronics, all with reviews on the state-of-the-arts and discussions about future developing trends, whereas the next two provide overviews on specific technologies, such as components, packaging and integration, and power converters etc., for almost all kinds of application areas.

We begin with a paper on the power electronics applications to electric vehicles. It is authored by Dr. Rik De Doncker and his research group from RWTH Aachen University. It provides an overview of emerging technologies for modular power converter architectures for electric vehicles. Technologies like wide-bandgap power semiconductors, smart topology enhancements, control methods, and highly integrated bidirectional battery charger systems with intelligent charging strategies are all discussed.

The second paper is about power electronics applications to the electrification of subsea systems. It is written

by Dr. Kaushik Rajashekara and his research group from the University of Houston. It presents a summary on the requirements and challenges in the power distribution and conversion for subsea systems, which have become more predominant in recent years. The issues that are discussed include power architectures, power system components, power converters and motor drives, and health analytics and fault handling.

The third paper is regarding the power electronics applications to distributed energy storage systems (ESS) for electric power utilities. It is written by Dr. Liuchen Chang and his research group from the University of New Brunswick. A review of the energy storage market and technology is presented, with a classification of ESS grid support functions, followed by a detailed evaluation on the power electronic converters for distributed ESSs.

The fourth paper introduces power electronics applications to mobile communication systems. It is written by Dr. Xinbo Ruan and his research group from Nanjing University of Aeronautics and Astronautics. The paper sorts, compares and summarizes all different kinds of envelope tracking (ET) power supplies for different specific modern mobile communication systems. Ideas including soft-switching, slow envelope, and band separation are also proposed as possible solutions to further improve the efficiency of the ET power supplies.

The fifth paper is written by Dr. Laili Wang, Dr. Xu Yang and their students from the Power Electronics and Renewable Energy Center at Xi'an Jiaotong University, discussing integration technologies for power electronics systems. It reviews and evaluates the state-of-art integration technologies, including an active integration part which covers interconnection, packaging structure, and packaging material for power semiconductor devices, and a passive integration part which encloses magnetic integration, electromagnetic integration, and low-temperature co-fired ceramic (LTCC) technology.

Last but not least, the sixth paper is written by Dr. Conor Quinn and Mr. Dhaval Dalal, both representing the Power Sources Manufacturers Association (PSMA). PSMA publishes a technical report called Power Technology Roadmap (PTR) every two years, supplying an in-depth review on the recent technological developments related to power sources. This paper summarizes the methodology used and the key findings captured in the most recent edition which was released in March 2017. I believe there is no better arrangement than having a paper like this, reflecting visions of so many technological leaders from power electronics industries, to conclude this Part 5 and the whole Special Issue as well.

I'd like to thank the authors of all these 6 invited papers. It's their high-quality contributions that finally leads to the launching of this new journal. I'd like to thank Dehong Xu, President of CPSS, who in 2015 initiated the idea of publishing the new journal and since then has been persistently supporting my work as the founding Editor-in-Chief. I'd also like to thank Jiaxin Han, Secretary General of CPSS, Jan A. Ferreira, President of IEEE PELS, 2015-2016, Don F. D. Tan, President of IEEE PELS, 2013-2014, and Frede Blaabjerg, IEEE PELS Vice President for Products, 2015-2018, who form the CPSS and IEEE PELS Joint Advisory Committee for our new journal with Dehong Xu and myself. Other IEEE officers and leading staffs like Dushan Borojevich, PELS President, 2011-2012, Alan Mantooth, PELS President, 2017-2018, Mike Kelly, PELS Executive Director, and Frank Zhao, Director of China Operations, IEEE Beijing Office, just to name a few, also provided continuous support and constructive advices. My earnest thanks also go to the CPSS Editorial Office led by Lei Zhang, Deputy Secretary General of CPSS, for their wonderful editing work. It would not have been possible to create a new journal in such a short time without their efforts. I'd like to finally thank all the members of the Executive Council of CPSS and particularly the leaders of Chinese power electronics industry. They always firmly stand behind CPSS TPEA and ready to help whenever needed.

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Jinjun LIU received his B.S. and Ph.D. degrees in Electrical Engineering from Xi'an Jiaotong University (XJTU), China in 1992 and 1997 respectively. He currently holds the position of XJTU Distinguished Professor of Power Electronics, sponsored by Chang Jiang Scholars Program of Chinese Ministry of Education, leading the Power Electronics and Renewable Energy Center (PEREC).

Dr. LIU coauthored 3 books (including a textbook), published over 200 technical papers in peer-reviewed journals and conference proceedings, and holds more than 30 invention patents (China/USA). He received for 7 times governmental awards at national level or provincial/ministerial level for scientific research achievements or academic/teaching career achievements. He also received the 2006 Delta Scholar Award, the 2014 Chang Jiang Scholar Award, the 2014 Outstanding Sci-Tech Worker of the Nation Award, and the IEEE Transactions on Power Electronics 2016 Prize Paper Award. His research interests are power quality control and utility applications of power electronics, micro-grids for sustainable energy and distributed generation, and more/all electronic power systems.

Dr. Liu has served as the IEEE Power Electronics Society (PELS) Region 10 Liaison and then China Liaison for 9 years, an Associate Editor for the IEEE Transactions on Power Electronics for 9 years, and starting from 2015 the Vice President for membership of IEEE PELS. He is on Board of China Electrotechnical Society (CES) and was elected to a Vice President of the CES Power Electronics Society in 2013. He is the Vice President for International Affairs, China Power Supply Society (CPSS) and the inaugural Editor-in-Chief of CPSS Transactions on Power Electronics and Applications.

Key Components of Modular Propulsion Systems for Next Generation Electric Vehicles

Alexander Stippich, Christoph H. van der Broeck, Alexander Sewergin, Arne Hendrik Wienhausen, Markus Neubert, Philipp Schülting, Silvano Taraborrelli, Hauke van Hoek, and Rik W. De Doncker

***Abstract*—The objective of this paper is to provide an overview of emerging technologies for modular power converter architectures for electric vehicles. Nowadays, the most common electrical drive-train architecture exhibits one single inverter which is directly tied to the battery. As a consequence, only one high-voltage battery module can be applied and the dc-link voltage of the inverter and its apparent power rating is directly dependent on the available battery voltage. To overcome this restriction, modern power converter architectures with a higher degree of freedom have been proposed. These architectures exhibit modular dc-dc converters to allow different battery technologies to be linked to drive inverters operating independently from each other. To make this development feasible, new components and technologies are evolving which enhance the efficiency over mission cycles while ensuring further integration of the power-converter architectures.**

Wide-bandgap power semiconductors enable high switching frequencies and miniaturization of passive devices. Smart topology enhancements and control methods allow a significant loss reduction, in particular at light loads, resulting in a higher efficiency of the drive train over the entire driving cycle. Highly integrated bidirectional battery charger systems with intelligent charging strategies inhibit battery degradation and provide opportunities for grid stabilization. It is demonstrated how these technologies are realized and implemented to contribute to the development of future electric vehicles.

***Index Terms*—Dc-Dc-Converters, drive train, electric vehicles, power electronics, system architecture.**

I. Introduction

THE unavoidable reduction of green-house gases [1] and the health threatening air pollution in urban areas [2] are major drivers for the extinction of combustion engines and the rise of electric drives as key component for any future transportation. To make this development economically feasible it is necessary to increase efficiency, reduce cost and weight of components and meanwhile improving the overall reliability of the propulsion system.

Nowadays, most electrical drive-train architectures exhibit a single high-voltage battery with more than 100 cells in series resulting into a nominal voltage rating of approximately 400 V [3]. The high-voltage battery is directly connected to the drive inverter [4], [5]. To enable domestic charging of the battery, a galvanically isolated single-phase unidirectional charger is installed within the vehicle. This architecture has the drawback that the battery voltage and dc-link voltage of the drive inverter are tied to each other. However, the most feasible voltage of the battery pack is not necessarily the perfect voltage for the drive inverter.

From the perspective of the battery pack, a modular and low battery voltage is a desirable design option. It allows to combine high-power and high-energy battery technologies in parallelized units as hybrid battery systems, which promises cost and weight reduction, as well as efficiency improvements in particular under light load conditions [6]–[8]. In addition, battery lifetime can be increased by using a lower battery voltage as this requires fewer cells to be connected in series where the spread in cell aging becomes less relevant [9]. Finally, using modular battery packs at extra low voltages below 60 V significantly reduces the potential hazards resulting from the battery system during production and maintenance or in case of an accident [8], [10].

In contrast to the battery, the inverter and electric machine can be operated most efficiently at an adjustable dc-link voltage with the aid of dc-to-dc converters [5,] [11], [12]. This is because the switching losses of the inverter can be significantly reduced by dynamic adjustment of the dc-link voltage as function of speed of the machine, which enables lower PWM switching frequencies, lower noise and even transition into six-step operation [13]. The required inverter voltage ranges from the proposed traction battery of, for example, 96 V to the common dc-link voltage for automotive inverters of 400 V or even higher. With the introduction of SiC power modules the dc-link voltage can be raised even higher from 400 V up to 800 V [14]. This higher voltage capability increases the power rating of power plugs of charging stations. Consequently, it allows to reduce the charging time of the battery as well as the current rating of the drive train by a factor of two [15]. The possibility to charge faster the battery on the one hand and weight and cost reduction on the other hand are important driving factors, which will continuously push the dc-link voltage of the inverter to the 800 V level.

Another component within the traditional power architecture, which is worth reconsideration, is the unidirectional charger. In the last years a lot of research has been pursued in the area of bidirectional charger systems typically based on the dual-active bridge (DAB) converter [16]. Bidirection-

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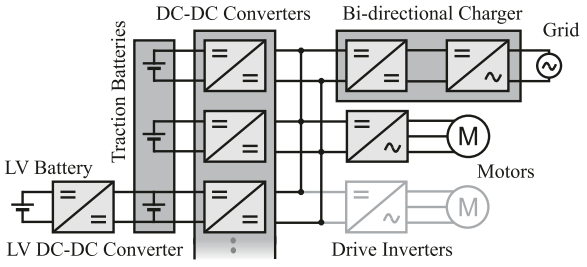


Fig. 1. Modular propulsion system architecture.

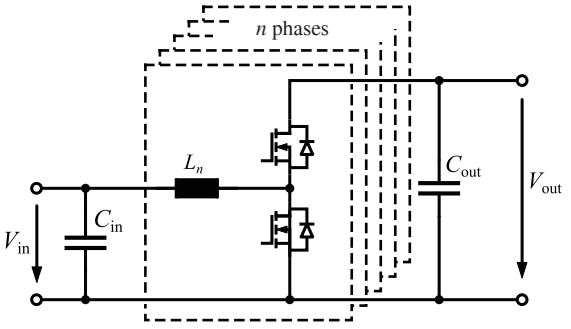


Fig. 2. Multi-phase boost converter.

al chargers allow to increase the lifetime of batteries with intelligent charging strategies by keeping the state of charge during night at an optimal level [17], [18]. Furthermore, they may support the grid via active and reactive power injection [18]–[20].

The presented arguments underline that a modular power converter architecture exhibiting dc-dc converters as dynamic link between battery units and the drive inverter is a promising solution. The decoupling of the battery voltage from the propulsion system voltae can contribute to a much more efficient operation and lower cost construction of the battery, the inverter and the machine. However, this additional component must pay off, as it adds weight, loss and cost.

This paper addresses the components and operation techniques which are necessary to realize a modular and highly efficient power-converter architecture. The assessment focuses on new devices and components which allow a strong miniaturization and cost reduction of the next generation dc-dc converters. Methods for smart loss reduction are presented to increase the efficiency of the proposed architecture in comparison to the traditional one. Finally, technologies for size and loss reduction of a bi-directional battery charger are illustrated.

II. Next Generation Power Converter Architecture

The proposed power-converter architecture depicted in Fig. 1 exhibits multiple modular traction batteries. Each battery is connected to a dc link via a dc-dc converter. The dc link supplies one or more drive converters and can be connected directly to the grid using integrated bidirectional battery chargers [18], [21]. The electrical system of the vehicle, which is typically operated at 12 V, is supplied via a low-voltage dc-dc converter connected to one of the traction batteries [22].

This topology has been developed and successfully validated within a full electric vehicle in the publicly funded projects *Europahybrid* [11] and *e performance* [23]. The biggest advantage of this propulsion system architecture is its modularity. Standardized battery units with integrated dc-dc converters, the so-called smart battery, can be stacked to provide a desired power and energy rating [12], [14]. Thereby, different drive trains can be realized using the same components which results in lower costs due to the economy of scale [5].

In most investigations, the dc-dc converters interfacing the batteries with the dc link are based on multi-phase boost converters [11], [14], [23]. This topology allows a very efficient and compact design, in particular if wide-bandgap power semiconductors are applied [14], [24]. However, given a rated dc-link voltage of 400 V the minimal battery voltage cannot be set below 100 V without jeopardizing the efficiency of the dc-dc converter. For this reason, it is also interesting to consider galvanically isolated topologies with buck-boost functionality, e.g. single or three-phase dual-active bridge (DAB) converters [25]. In case of a galvanic isolation, two 48 V battery cells can be connected in series to a total of 96 V, with the middle potential tied to the vehicle ground potential like proposed in [5]. Thereby, the entire power converter architecture can rapidly discharge the dc-link bus to ensure that the entire electrical system is intrinsically safe. However, the galvanically isolated converter requires a high-frequency transformer that may add additional losses and weight.

III. Non-Isolated Dc-Dc Converters

The multi-phase boost converter as shown in Fig. 2 is a promising topology for non-galvanically isolated dc-dc converters which interface a high-voltage battery at, e.g. 400 V, and the drive inverter at a dc-link voltage up to 800 V. It shows high efficiency over the entire output power range when intelligent phase-shifting and phase-shading is applied [14]. Fig. 3 shows a typical efficiency plot for a multi-phase approach with and without phase-shading. Especially at light-load conditions, the efficiency can be increased significantly if a number of phases are turned off corresponding to the required output power. As electric drive trains in EVs are often operated at partial load, the light-load efficiency is an important design criteria of such power converter systems [14].

On the one hand the multi-phase approach is perfectly suited for modular power converters as the output power is scalable by selecting the number of required phases. Furthermore, the parallelization can lead to improved economies of scale.

On the other hand, multiple phases result in higher control complexity and higher costs for additional driver circuitry and sensors. Moreover, the volume occupied by the current sensors and the gate drivers has to be considered. Commercially available gate drivers are often not suitable as they do

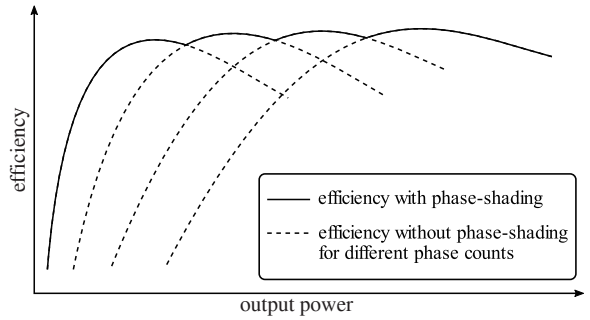


Fig. 3. Typical efficiency plot for multi-phase boost converters with and without phase-shading [14].

not fulfill power density requirements. Therefore, custom and low cost gate drivers have to be designed which fit in the given space.

A. Advantages and Challenges of Wide-Bandgap Devices

In terms of weight, size and cost, dc-dc-converters for electric vehicles can profit significantly from the application of wide-bandgap (WBG) semiconductors like silicon carbide (SiC) and gallium nitride (GaN). They show superior switching characteristics that allow the designer to raise switching frequencies by at least one decade.

Moreover, all dc-dc converters require passive devices for filters and energy storage. These passive components can be dimensioned smaller with increasing switching frequency, reducing weight, size and cost of the overall system [24], [26]. Despite the higher prices of WBG semiconductors in comparison to silicon semiconductors, the overall system cost in WBG based power converters can be reduced significantly due to the size reduction of passive devices. The smaller the size, the less cost intensive materials like high-performance ferrite, copper or litz-wire are required [24]. In addition, the higher power density results in a reduced weight of the drive train and thus contributes to a higher driving range of EVs.

With increasing switching frequencies the design of passive components, particularly magnetic components, becomes more challenging. Especially in converters with GaN devices, which can operate at elevated MHz switching frequencies, the magnetic components often enforce a limit on the total power density, because the magnetic losses can not be dissipated easily [26]. To overcome this issue, sophisticated designs of high-frequency magnetic components must be pursued by intensive research [24].

High switching frequencies are also challenging regarding current sensing. Using a multi-phase boost converter, the current of each phase has to be monitored and must be controlled with high bandwidth to ensure a balanced current distribution between all phases. Therefore, current sensors with a high bandwidth are required to sample currents at these elevated switching frequencies. The bandwidth of the current sensors must be at least one decade above the switching frequency of the converter, such that the phase delay between the actual current flowing in the phase and the measured current is minimized. This is important because a large phase delay leads to less time for the processing of the measured data and the computation of the control algorithms.

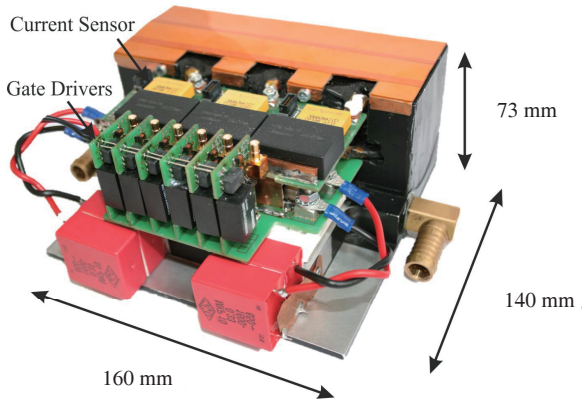


Fig. 4. 3-phase SiC-based boost converter prototype without copper busbars and common mode chokes.

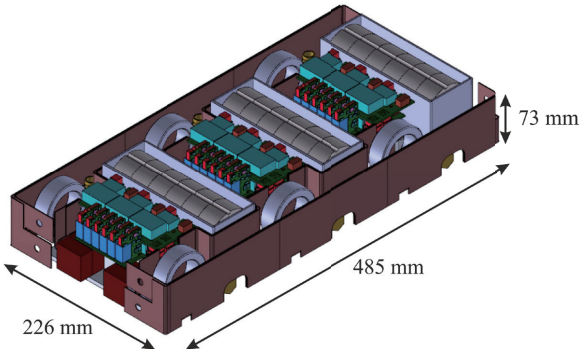


Fig. 5. CAD-model of a 9-phase SiC-based buck-boost converter consisting of 3 converter building blocks, resulting in 126 kW peak power.

B. Comparison between Si and SiC based converters

Fig. 4 gives an example for a compact SiC dc-dc power-converter building block [14]. It consists of a 3-phase buck-boost converter with a power density of 43 kW/dm^3, a displacement volume of 0.98 dm^3 and a switching frequency of 150 kHz. The main benefit of this dc-dc converter is its modular approach. The converter building block with a peak output power of 42 kW can be used standalone or in a parallel configuration (see Fig. 5). Thus, the maximum output power is scalable in steps of 42 kW.

The key benefit of SiC-based dc-dc converters becomes obvious in comparison to a representative Si-based converter of the same topology with six phases (see TABLE I). The mentioned Si-based converter with a power density of 6.9 kW/dm^3 and a switching frequency of 16 kHz is shown in Fig. 6. Efficiency measurements of the two dc-dc converters are given in Fig. 7 for a power of up to 42 kW. Both converters, the Si and the SiC converter, are operated under hard switching conditions. The switching frequency f_{sw} of the SiC converter is nearly a decade higher than of the converter with Si devices. Nevertheless, the overall efficiency

TABLE I
COMPARISON OF SI AND SIC DC-DC CONVERTER

Parameters	Si DC-DC Converter	SiC DC-DC Converter
Semiconductor	Si-IGBT(650 V)	SiC-MOSFET (1200 V)
Power per phase	40 kW	14 kW
V_{in}	120-280 V	80-500 V
V_{out}	max 400 V	max 900 V
f_{sw}	16 kHz	150 kHz
Power density	6.9 kW/dm^3	43 kW/dm^3

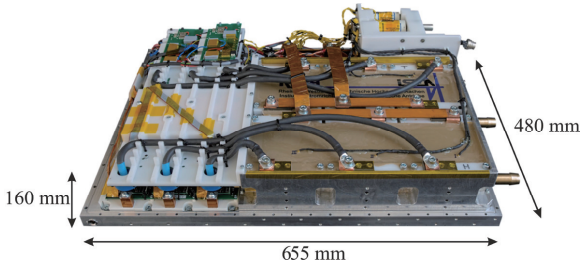


Fig. 6. 6-phase Si-based dc-dc converter with 240 kW peak power, 35 dm^3 displacement volume [23].

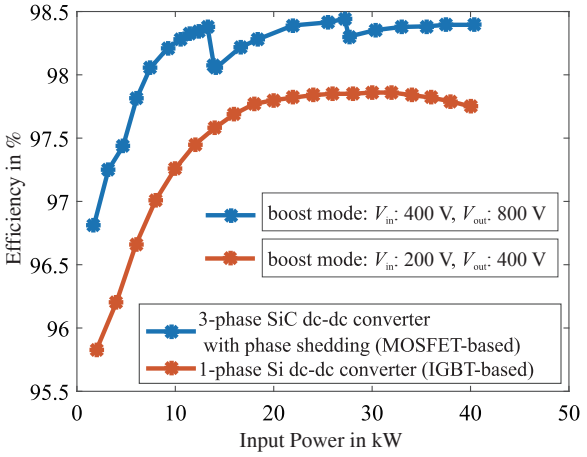


Fig. 7. Efficiency comparison of the 3-phase interleaved SiC converter building block and 1 phase of the 6-phase Si dc-dc converter.

of the SiC based converter is higher over the whole operating range. The reason is the relatively low switching loss which is inherent to SiC devices while the more fine-grained phase-shading additionally increases light-load efficiency. The SiC based converter also exhibits a power density increase by a factor of six.

IV. GALVANICALLY ISOLATED DC-DC CONVERTERS

Galvanically isolated dc-dc converters can be used in different parts of the drive train to realize high voltage conversion ratios or to increase safety. An example for such a converter is the interconnection of the HV drive train with the 12 V power system, see Fig. 1. The galvanic isolation is implemented with a high-frequency transformer, which

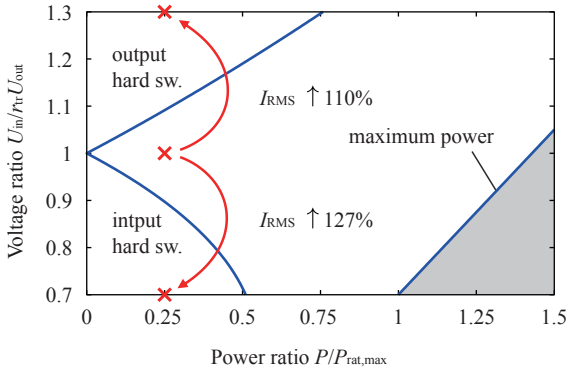


Fig. 8. Exemplary soft-switching boundaries and changes of RMS current of a single-phase DAB converter.

commonly requires a higher effort, particularly more power semiconductors, and a more sophisticated operation scheme compared to a galvanically coupled converter. This brings additional complexity, size, weight and cost to the power converter. Accordingly, efficient and compact converter concepts with high switching frequencies and a carefully designed transformer are essential.

The dual-active bridge converter [25] is one of the most promising galvanically isolated dc-dc converters as it offers a fully bidirectional power transfer, a low number and small size of passive components and a good device utilization [27]. Furthermore, the phase currents and the output currents of the converter can be seamlessly adjusted within less than one switching period resulting in a highly dynamic control of the power flow using a feed-forward control [28], [29].

Dual-active bridge converters are capable of achieving zero-voltage switching (ZVS) over the whole operating range at equal port voltages [25]. Fig. 8 shows typical zero-voltage switching (ZVS) boundaries of a dual-active bridge converter as a function of the voltage ratio and the output power, where U_{in} is the input voltage, U_{out} the output voltage, r_{tr} the transformer turns ratio, $P_{\text{rat,max}}$ the maximum rated power and I_{rms} the RMS current in the transformer. The boundaries are determined by the design of the converter, i.e., the leakage inductance and the switching frequency, and are strongly influenced by the dead time, the magnetizing current and the output capacitance of the semiconductors [22], [27], [30]. Obviously, the dual-active bridge converter suffers from large hard-switching areas at unequal voltage ratios diminishing the efficiency of the converter. In addition, during hardswitching operation a significant increase of the RMS current in the transformer can be observed, which particularly reduces the efficiency at low to medium powers depending on the covered voltage range [22].

A. Modulation Strategies

In order to minimize the hard-switching area and the RMS currents of the dual-active bridge converter, sophisticated operation strategies have been developed for the single-phase dual-active bridge [22], [27], [31]. Those so-called

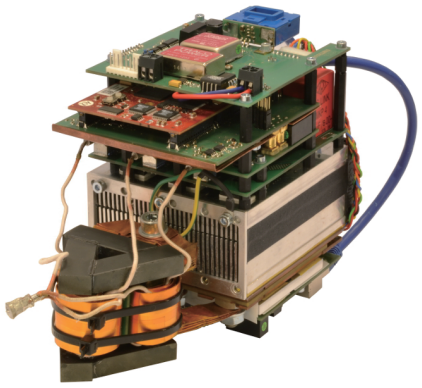


Fig. 9. Photograph of an air-cooled, galvanically isolated three-phase dual-active bridge dc-dc converter. Volume with housing around 2.4l.

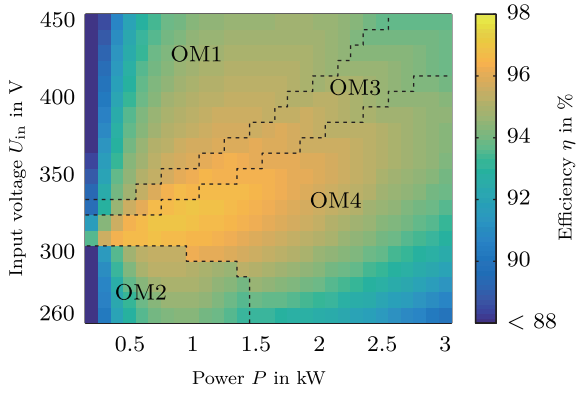


Fig. 10. Efficiency of a three-phase dual-active bridge converter using optimized operation strategies (simulation results).

dual-phase-shift operation strategies utilize the zero-voltage state of the input and output bridges to ensure softswitching over the whole operating range. Among the proposed operation strategies, the triangular and trapezoidal current-mode are most promising as they offer low RMS currents and near zero-current switching over a wide operation range [31]. These operating modes can also be enhanced to achieve zero-voltage switching [22]. This enables converter efficiencies between 90% and 98% over a wide voltage and power range.

To further boost maximum efficiency, three-phase dual-active-bridge topologies can be used [31]. Similar to galvanically coupled dc-dc converters, the interleaved operation of multiple phases results in reduced filter size [22]. Multi-phase dual-active bridge converters, however, cannot be operated efficiently over a wide voltage range using the standard single phase-shift operation [25]. Consequently, auxiliary circuits [32] and multilevel topologies have been investigated to improve the soft-switching range and the efficiency [33]. Furthermore, the so-called parallel-phase operation [22], [34], [35] and the duty-cycle operation [36] have been developed. Those operation strategies allow to utilize the dual phase-shift operation strategies known from the single-phase dual-active bridge by either changing the phase shift between the switches of each port or by utilizing

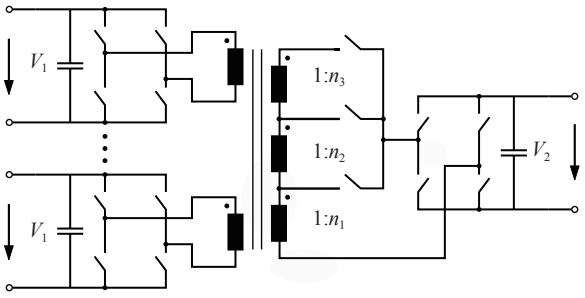


Fig. 11. Dual-active bridge converter with tap changer.

an asymmetric duty cycle. This possibly diminishes some advantages of the multi-phase dual-active-bridges and, therefore, requires a careful design of the converter [22], [35].

Fig. 9 shows the photograph of a highly integrated three-phase dual-active bridge dc-dc converter with a rated power of 3 kW and a switching frequency of 100 kHz [22]. The converter interconnects the low-voltage battery (nominal voltage of 14 V) and the high-voltage dc-bus (260 V-450 V), cf. Fig. 1. Despite the galvanic isolation and the low output voltage which results in currents of up to 215 A, measured efficiencies of more than 96% have been reached [22]. Different operating modes are used (see Fig. 10), which also includes a variation of the switching frequency. Measurements proof that the majority of the operation range can be covered with efficiencies of more than 92% while a mean efficiency of 93.5% is reached, which is quite unique given the wide voltage range. The dual-active bridge converter can be easily utilized as a power-electronic building block allowing for easy scalability towards higher powers [27], [37].

B. Dual-Active Bridge Converter with Tap Changer

The combination of a dual-active bridge converter with a tap changer as outlined in Fig. 11 allows to operate the dual-active bridge converter with high efficiency over an exceptionally wide operating range. This concept has been studied with a single-phase dual-active bridge converter which enables the usage of a low-voltage battery (30 V to 60 V) in an HV traction system with a dc-link voltage between 100 V and 400 V [38]. This way, the aforementioned improved safety, redundancy and performance of low voltage batteries can be utilized in combination with a variable dc-link voltage for higher inverter efficiency.

The transformer with tap changer is introduced to adapt the winding ratio according to the input and output voltages. This enables a converter operation close to unity voltage ratio throughout the whole operating range, which leads to higher efficiencies [38], [39]. Fig. 12 depicts the power losses of a single-phase dual-active bridge converter at different winding ratios n. It can be seen that the power losses at light loads can be significantly reduced when the turn ratios $n = 3$ to $n = 7$ (cf. Fig. 12(a)-12(c)) are chosen optimally for each operating point (see Fig. 12(d)). This is due to the increased soft-switching area as indicated in Fig. 8 as well the reduced RMS currents.

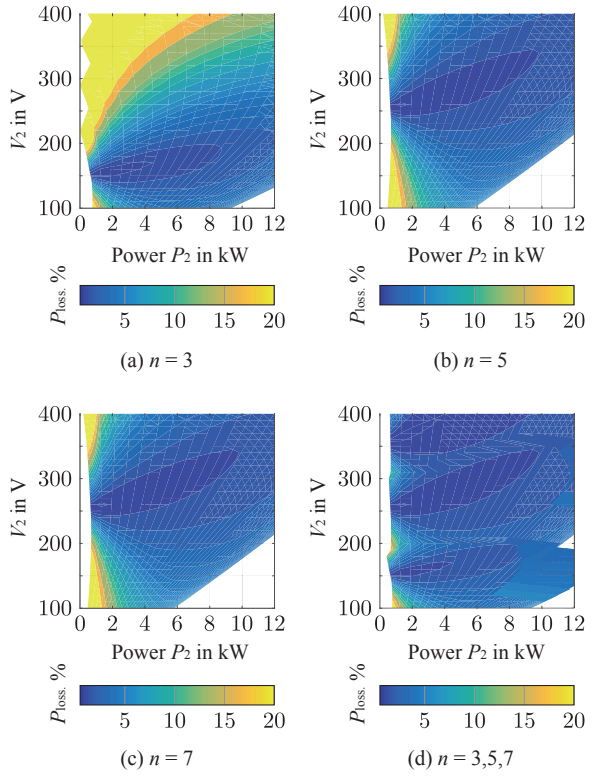


Fig. 12. Power loss with different tap configurations.

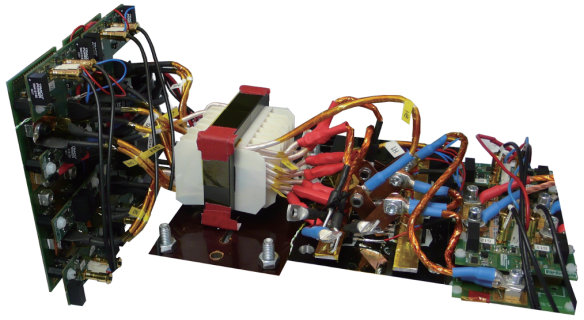


Fig. 13. Photograph of a 10 kW laboratory prototype of a single-phase dual-active bridge converter with tap changer [38].

Ultimately, the number of taps added to the transformer is a trade-off between efficiency and increased system complexity. Each tap requires additional components to switch between the different taps of the transformer. This can be realized with either relays, thyristors, IGBTs or MOSFETs. The devices must be selected based on the application as each device is a trade-off between cost, size, dynamic behavior and conduction losses of the tap changer. However, remaining hard-switching areas of the converter can still be eliminated by changing the modulation strategy as outlined previously, for example with the triangular modulation.

The design of a transformer with tap changer is more challenging in comparison to the design for a standard transformer of a dual-active bridge converter. The transformer must be coiled with regard to similar stray inductances. Therefore, the magnetic coupling between all windings must be very similar to obtain a uniform current distribution between the windings. As a result, the magnetic induction in the ferrite has to be kept relatively low and the transformer has its maximum efficiency at low load and not around the middle of its power range.

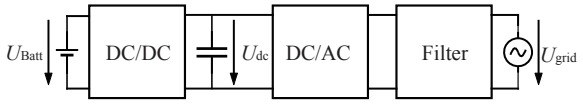


Fig. 14. Topology of a two-stage battery charger.

TABLE II
MEASURED EFFICIENCY AT DIFFERENT TAPS WITH TURNS RATIO n AT $V_1 = 50$ V

$n = 3$		$n = 5$		$n = 7$	
V_2 = 150 V		V_2 = 250 V		V_2 = 350 V	
P_2 in kW	η in %	P_2 in kW	η in %	P_2 in kW	η in %
0,391	93,8	0,469	94,1	0,787	96,4
0,745	96,4	0,839	96,8	2,316	96,4
2,084	95,3	2,220	96,2	4,683	95,3
3,087	94,3	3,343	95,8	5,690	94,7
3,975	93,1	4,373	95,0	6,660	94,2
4,751	91,8	5,261	94,1	7,522	93,8
		6,113	93,2	8,225	92,2

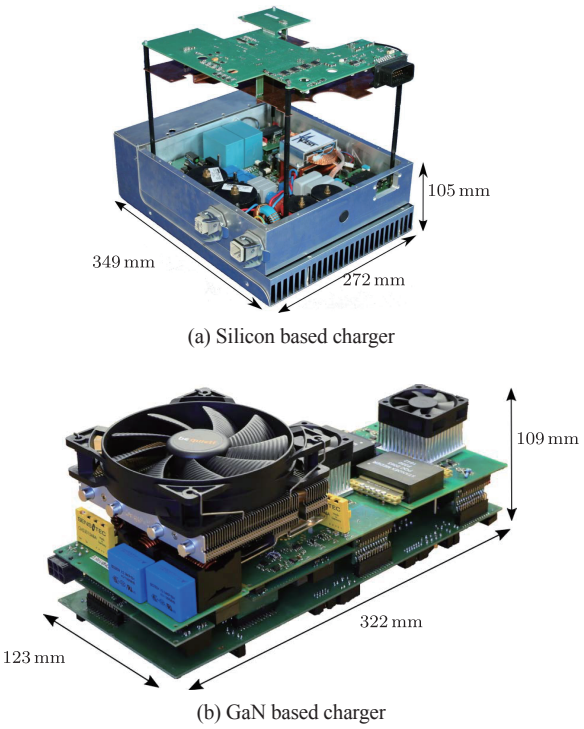
Fig. 13 shows an image of a laboratory prototype of a single-phase dual-active bridge converter with a tap changer, a power rating of 10 kW and a switching frequency of 100 kHz. The low voltage (30 V to 60 V) H-bridges can be seen on the left side. To handle the high currents in the LV port and to optimize the current distribution in the transformer, several H-bridges are connected in parallel. Moreover, the presence of multiple H-bridges also allows to connect different battery packs. The transformer and the MOSFET based tap changer are visible in the middle of the photograph. The high-voltage H-bridge which is implemented with SiC MOSFETs is shown on the right side.

Efficiency measurements of the converter are listed in TABLE II. The converter achieves an efficiency between 91.8% and 96.8% using only standard single phase-shift modulation. To further improve the efficiency, more sophisticated modulation strategies like the triangular or trapezoidal modulation mentioned above can be applied.

V. GRID-TIED BATTERY CHARGERS

In this section, concepts and technology trends for a compact and efficient on-board charging unit are discussed. The most common type of on-board charging systems are single-phase grid-tied chargers that exhibit a power rating of 3.7 kW to recharge the electric vehicle at any household.

Today, most chargers allow only an unidirectional power flow. Consequently, the battery can be charged from the



(a) Silicon based charger

(b) GaN based charger

Fig. 15. Comparison of a Silicon and a GaN based battery charger.

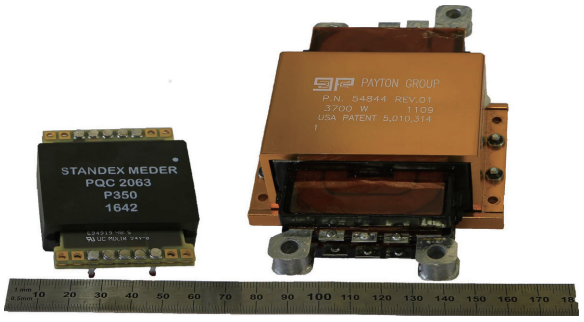


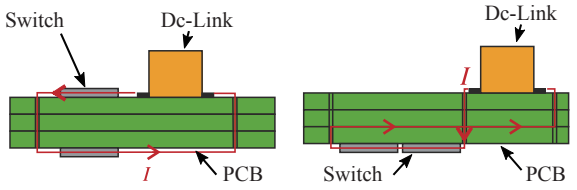
Fig. 16. Comparison of a 500 kHz transformer (left) and a 50 kHz transformer (right) for a power rating of 3.7 kW.

grid but cannot feed energy back into the grid. Bidirectional chargers enable an energy flow in both directions. This can be used to utilize the batteries within the electric vehicles as a large distributed energy storage unit to buffer the fluctuating energy produced by wind and solar power plants, at least, if a significant number of electric vehicles is equipped with such chargers [19]. Furthermore, a bidirectional charger can increase the lifetime of the battery by using intelligent charging strategies which keep the average state of charge (SOC) of the battery at an optimum level during standstill. Despite the increased number of power cycles, the calendaric aging which is directly related to the SOC is significantly reduced and, thus, the lifetime of the battery is enhanced [17], [18].

As the battery charger is commonly implemented inside the electric vehicle, it adds to the overall weight of the vehicle and must be built as small as possible. In case of bidirectional battery chargers, a two-stage topology with a discrete dc link as shown in Fig. 14 is proposed. This way, the inverter tied to the grid and the dc-dc converter connected to the battery can be optimized independently.

TABLE III
DIMENSIONS OF BOTH BATTERY CHARGERS

	Width	Length	Depth	Volume	Power Density
Silicon	272 mm	105 mm	349 mm	9.9 l	370 W/l
GaN	123 mm	109 mm	322 mm	4.3 l	860 W/l



(a) Stray inductance of 3.24 nH

(b) Stray inductance of 2.78 nH

Fig. 17. Stray inductances as a result of different layouts.

The bidirectional dc-dc converter can be realized by a galvanically isolated single-phase dual-active bridge converter, see Section IV. The dc-link capacitor exhibits a power ripple with twice the grid frequency. This power ripple must be buffered by the dc-link capacitor. However, a large capacitor significantly adds to the overall size of the charger [40]. Another solution is to completely apply the power ripple to the battery [41].

A. Battery Charger with Wide-Bandgap Devices

The advantages and challenges when utilizing GaN devices for battery chargers [42] are quite similar to those outlined in Chapter III-A. For example, passive devices like the transformer of the dual-active bridge converter can be reduced in size and weight. Fig. 16 shows two planar transformers for a switching frequency of 50 kHz and 500 kHz at the same power rating. The size of the transformers are 344 cm^3 and 58 cm^3, respectively. Due to the increased switching frequency, the volume of the transformer can be reduced by 83%.

The switching frequency of battery chargers, however, is often set below 50 kHz to keep the third harmonic below 150 kHz. As a consequence, the third harmonic of the switching frequency, which cannot be eliminated by choosing sophisticated modulation schemes, does not have to be damped due to CISPR-14 regulation and, thus, eases filtering. However, it was demonstrated, that higher switching frequencies allow to reduce the size of the grid filter components even if the switching frequency itself must be damped. By choosing a switching frequency of 500 kHz the size of the grid filter of a bidirectional charger (cf. Fig. 15(b)) could be reduced by 76.4%. This is because the resonance frequency of the grid filter can be chosen much higher due to the high switching frequency.

The mentioned GaN based charger with a nominal power of 3.7 kW and a switching frequency of 500 kHz is depicted in Fig. 15(b). It is air-cooled and has a power density of about 900 W/l. Fig. 15(a) shows a photograph of a Si based battery charger with the same power rating. The corresponding dimensions are listed in TABLE III. The overall volume of the GaN based charger is lower by 5.6l, yielding a power-density increase by a factor of 2.3. This illustrates the miniaturization and integration potential of GaN devices.

B. Challenges of GaN devices

At switching frequencies of 500 kHz a careful selection of passive components is important. For example, dc-link film capacitors exhibit a resonant frequency close to the switching frequency and are therefore not suitable. Ceramic capacitors pose a viable alternative.

Furthermore, the layout of the converter board, especially the switching cell, must be designed to achieve low stray inductances in the commutation path, cf. Fig. 17. The package of the GaN devices must also be selected for low stray inductance. At 500 kHz, even several nH of stray inductance will cause high over voltages which increase the switching losses and, hence, limit the switching frequency.

To reduce the switching losses, the switching speed of the GaN devices should be as fast as possible. As a consequence, a high voltage gradient up to 100 kV/µs occurs which causes common mode currents in the parasitic capacitances throughout the system. Thus, devices such as the galvanically isolated gate driver must feature minimal coupling capacitances to limit common mode currents.

As the size of GaN devices and packages is considerably smaller than of Si devices, cooling becomes more challenging. Due to the increased heat-flux density, the heat must be dissipated by means of heat spreading. Packages with top-sided cooling allow a direct attachment of heat sinks. Yet, galvanic isolation must be provided, e.g., by a direct copper bonded substrate. Consequently, the substrate can be soldered to the top side of the GaN devices, providing galvanic isolation and heat spreading. A suitable heatsink can then be soldered onto the other side of the substrate to dissipate the heat.

Overall, GaN devices impose new challenges on the design of converter systems. Nevertheless, it is anticipated that they will play a key role to build small yet highly efficient converters for future automotive applications.

VI. Conclusions

A modular power-electronic architecture for future electric vehicles was proposed which decouples the battery voltage from the dc-link voltage of the machine inverter. The key components of the architecture, namely the dc-dc converters and the battery charger, have been outlined.

If no galvanic isolation is required, multi-phase boost converters in combination with wide-bandgap devices enable small and highly efficient dc-dc converters. For improved safety and reliability, galvanic isolation can be easily included within the architecture. In this case, the dual-active bridge converter is perfectly suited as it provides a bidirectional power flow and requires a minimum amount of additional passive devices. Efficiency issues at lowload conditions have been solved using various approaches. Last but not least, the utilization of bidirectional battery chargers with intelligent charging strategies is endorsed to enhance lifetime of battery cells. In combination with wide-bandgap devices, the size of passive devices including the line filters can be significantly reduced resulting in highly-integrated and efficient battery chargers.

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Electrification of Subsea Systems: Requirements and Challenges in Power Distribution and Conversion

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***Abstract*—The subsea industry has become more predominant in recent years because of the discovery of a significant number of new oil and gas fields located in deep water, a term often used to describe offshore projects located in water depths greater than 600 feet. In order to extract oil and gas, a large number of electrical systems need to be deployed at the seabed. Many of these electrical systems need high-reliability power grid and power control units located on the seabed to minimize downtime. Power system and power electronics play a major role in providing the required and reliable power to various electrical systems. But there are many challenges for deploying power components under the seabed. This paper presents the challenges and the requirements of power system components operating in subsea environment, use of power electronics for efficient transmission of power from the offshore platform or from the shore to the subsea electrical loads; variable speed drive systems; and research areas related to power electronics for subsea electrical systems.**

***Index Terms*—Architecture, HVDC transmission, power cables, power electronics, subsea power system, under water systems.**

I. Introduction

THE term subsea refers to the exploration, drilling, and development of oil and gas fields in deep water locations. These deep-water production systems require long distance power transmission and distribution that supply electrical power to various subsea loads from the onshore generating plants. Until recently, the offshore industry preferred placing the converters and power system equipment for supplying the subsea loads on shore or on the subsea vessel at the topside of the ocean. This was mainly because it is challenging for humans to install equipment at the bottom of the ocean due to harsh environments. With advancements in robotics and other technologies such as Autonomous Underwater Vehicles (AUVs), it has become possible to install more and more equipment on the seabed [1]. There are several advantages to installing power converters and equipment close to the loads. When the electrical converters and distribution systems are placed on the seabed, it considerably reduces the cost of the power supply with similar reliability. Thus, the offshore industry is now seeing a clear trend for production equipment to be installed on the seabed [2], [3].

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The installation and operation of subsea electrical systems have various challenges. The pressure increases by 10 bars (about 145 PSI) for every 100 m depth in the ocean. The electrical systems need to be located at a water depth of about 3000 m, which accounts for 300 bar pressure. At these depths, all the electrical components have to be designed and qualified to withstand high pressures. Additionally, sea water is a conductor and corrosive, hence proper isolation between the electrical equipment and the sea water needs to be provided. As the equipment is located at depths of up to 3,000 m, in the event of fault, maintenance will be a challenging and will not be possible without bringing the equipment to the surface. However, bringing the equipment to surface is expensive and can result in long production outages. Hence, the reliability of the equipment for the subsea applications has to be strictly designed for more than 20 years, which implies that the mean time between failures (MTBF) should be greater than 20 years. The mean time to repair (MTTR) for subsea systems is usually very long [4].

The equipment or systems such as electric submergible pumps (ESPs) and compressors used in the production and processing of oil and gas require large amount of electrical power which is of the order of 10-15 MW. Some of the existing systems adopt supply of electric power from large gas turbine generators, which are installed on fixed or floating platforms [5]. Because of the economic and environmental constraints involved in generating large amount of power on the platform and construction of the platform itself, there is an increasing tendency to move towards supplying power to the processing loads from the conventional onshore power plants using long distance power transmission cables. This can minimize cost and maintenance involved in the platforms. However, the long step-out distances of the order of 100 km have several problems related to reactive power compensation and the increased power umbilical size if HVAC power transmission and distribution systems are adopted [6]-[8]. Additionally, the voltage levels used for the subsea power transmission can be typically of the order of 36 kV to 100 kV. Power umbilical and the corresponding power components such as connectors and the penetrators have to be rated for such voltage levels. Type of power transmission used, whether AC or DC, could be decided by the power transmission distance based on the reactive power drawn from the source. Especially in subsea applications, each type of transmission system (AC and DC) has its own advantages and limitations which are discussed in the following sections.

Designing power electronic systems such as inverters for variable speed drives, power supplies, etc. for seabed and downhole applications is challenging. These systems have to operate

reliably under harsh environments, be easily repairable in case of any failure, and operate at high pressure environment and high temperatures with space limitations (downhole). At present, the power converters are assembled at atmospheric pressure in steel vessels. At larger sea depths, the wall thickness of the pressure vessel increases resulting in problems of heat transfer from the power converter to sea water. This also increases the total weight. Research is being pursued by only a few organizations to develop pressure tolerant power converters and associated gate drivers to reduce weight and volume [1].

This paper discusses many of the challenges and limitations involved in the power transmission, distribution, and electronic systems. Various power transmission and distribution architectures along with the possible considerations of HVDC transmission in the subsea industry are investigated. The advantages and limitations of AC or DC distribution for subsea systems are presented. A comprehensive review on various power components such as pressure tolerant power electronics [9]-[12] variable speed drives, high voltage circuit breakers, power umbilical [13]-[15], wet-mate connector, and penetrators used in the transmission system is presented. The paper also presents the requirements and challenges of subsea power electronic systems and possible power converter topologies.

II. Subsea Power Transmission and Distribution Architectures

The electrical power for the subsea industry is generated in two different ways, one being the offshore power generation and other is onshore generating station. In the case of offshore power generation, gas turbine driven generators are installed on the platforms that are located near the load. As the subsea loads such as ESPs and compressors are located very far from the onshore generating stations, it requires a long tieback power transmission system. Subsea industry has already started using high power high voltage AC transmission systems in order to minimize the power losses, and the reactive power due to the large capacitance of the power umbilical [16], [17]. The high voltage direct current (HVDC) transmission system in the subsea industry is being considered as an efficient power transmission solution for the long tieback subsea power systems as the number of power conductors and the reactive power consumption are minimal [18]. The transmission distance for a typical long tieback system spans from 100 km to 150 km and the distribution line distance is about 3000 m. The transmission voltages are typically kept at higher values, of the order 36 kV - 100 kV to compensate for the transmission power losses and also to reduce the reactive power consumption. However, the distribution line voltages are in general kept low of the order 3.3 kV to 6.6 kV, to supply the individual electrical loads. The HVAC systems employ line frequency bulk transformers at the sending and receiving ends of the transmission line as well as in the distribution systems. This results in a large footprint and low power density system.

A. HVAC Subsea Power Architectures

A typical HVAC subsea power transmission and distribution architecture is shown in Fig. 1. The subsea power system components are categorized as motors, power electronic converters, step up/down transformers, switchgear, uninterruptable power supplies (UPS), subsea control modules, power management systems, etc. It also consists of compressors and pumps for artificial oil lifting. Several subsea power architectures have been reported in the literature based on the AC configuration as shown in Fig. 2(a) and Fig. 2(b). In the HVAC subsea power architecture as shown in the Fig. 2(a), power for the subsea loads is generated on-shore. In order to reduce the transmission line power losses, the generator bus voltage is boosted to a higher value by using a step up transformer. The power architecture shown employs a variable frequency drive (VFD) in the transmission system for achieving soft-start of the transmission. It may also be noted from the Fig. 2(a) that this architecture employs a large number of line frequency transformers. As a result, the overall footprint becomes large. In addition, the distribution transformer used for interfacing the transmission system to the distribution system is a large line frequency transformer. To make the distribution hub a modular structure, a series connected open end transformer based ring architecture is reported in [19] as shown in Fig. 2(b). Main advantage of this architecture is that the distribution side transformers are specifically categorized to individual loads and the entire transmission line voltage is distributed among the transformers of lower rating. The main drawback of AC transmission and distribution system is the reactive power loss. The charging current, as a result of the large capacitance, is very high especially for the subsea power umbilical. This draws large amount of reactive power from the generating station, and results in higher power losses.

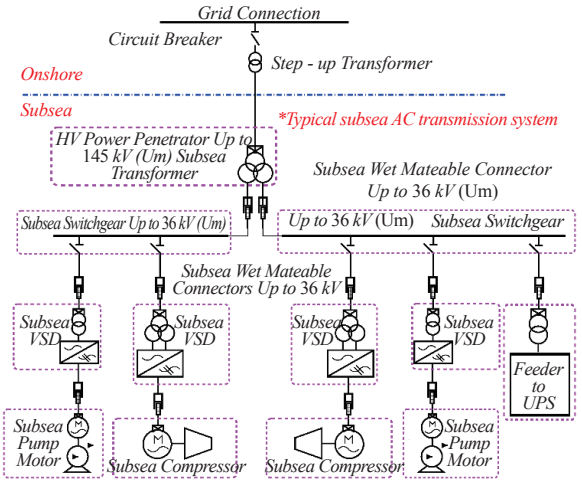

Fig. 1. Subsea power system block diagram.

B. HVDC Subsea Power Architectures

The HVDC power transmission has already gained importance in land based applications due to its advantage of enabling secure and stable operation of asynchronous interconnection of power networks that operate at different frequencies, precise and instant control of power, and zero reactive power consumption. In the conventional power transmission systems, it has

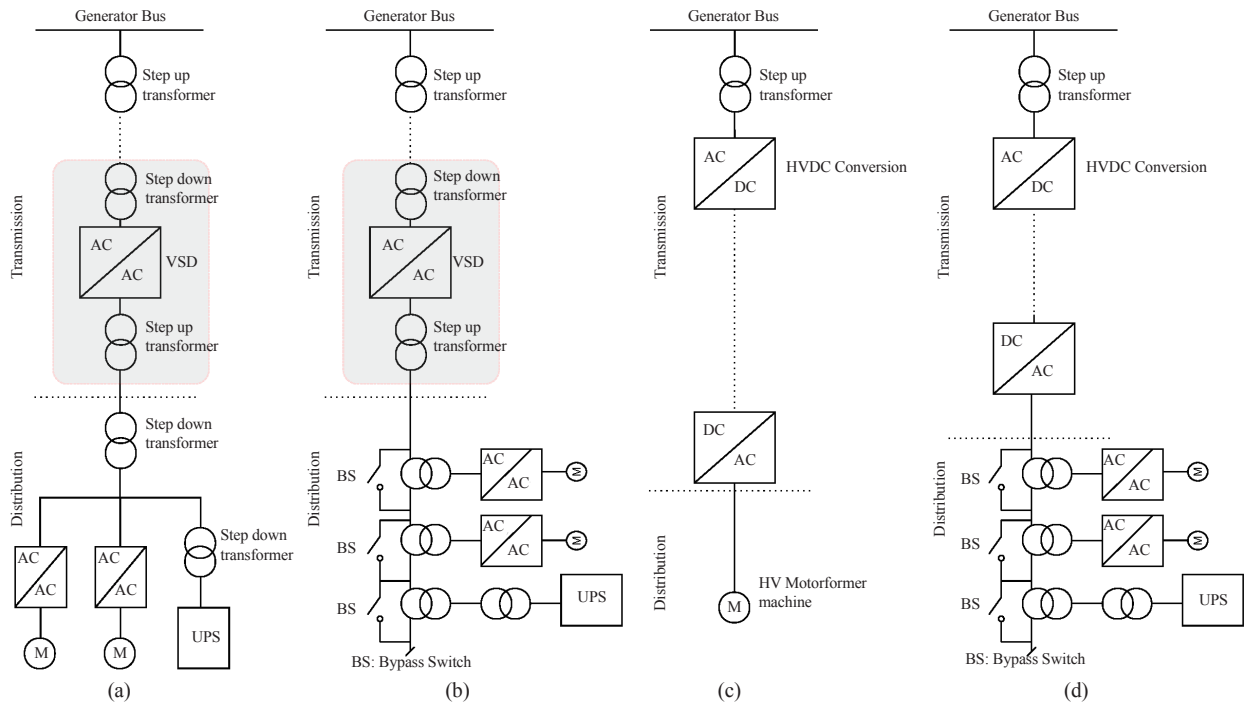

Fig. 2. Single line diagrams of various subsea power architectures, (a) HVAC subsea architecture [17], (b) Subsea HVAC ring type architecture [19], (c) Subsea HVDC power architecture of Troll A [18], (d) Subsea HVDC power architecture based on ring systems [19].

been found that the HVDC transmission overcomes HVAC systems for the transmission distances over 550 km. However, in underground and subsea applications, a few studies have shown that the breakeven distance reduces to about 50 km, considering reactive power compensation. The HVDC transmission shows improvements for step out distances greater than 50 km, as cable capacitance in the subsea power umbilical is significant [20].

Due to the advantages provided by HVDC transmission, there have been a few attempts to develop HVDC architectures for subsea application. Troll A, a production platform in North Sea based on the HVDC transmission is shown in Fig. 2(c), has a step-out distance of 70 km and at a water depth of about 300 m. It may be noted that the AC voltage generated at the platform is converted to a high voltage DC and the power is transmitted over a long distance via DC cables which has lower shunt capacitances, resulting in lower power losses. The HVDC is converted back to AC by using a power electronic converter that drives a high voltage 'motorformer' machine. The receiving end inverter is kept on a platform which is huge in size. Realizing Troll A configuration in the subsea environments will not be feasible due to its size. An attempt to further reduce the footprint and achieve modularity, a ring based HVDC structure as shown in Fig. 2(d) is been reported in [19]. This structure employs series connected open ended transformers at the distribution station, wherein each distribution transformer supplies power to the load individually. The HVAC voltage converted at the inverter (DC/AC) stage is distributed among multiple transformers and achieves modularity. In case of fault on a particular load, that particular section can be isolated by using a bypass switch which is connected across the primary winding of the transformer.

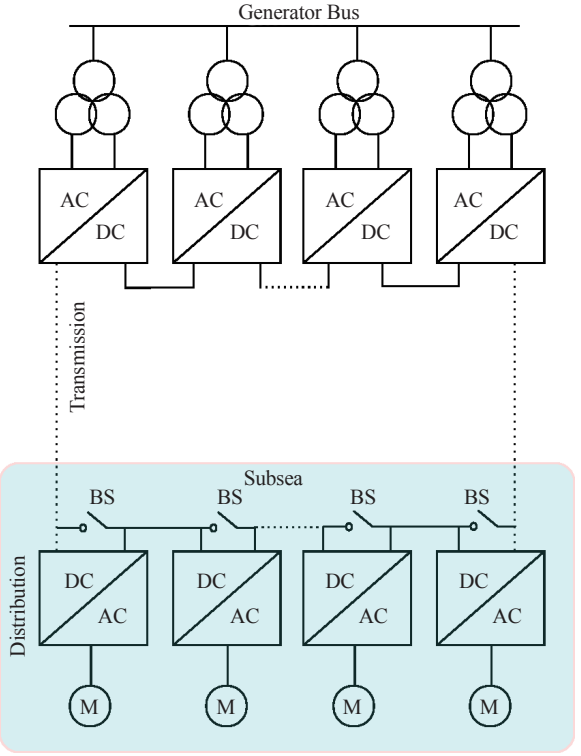

Fig. 3. Subsea modular stacked direct current structure [8].

Many subsea HVDC structures have been reviewed in [8], [19] with their merits and demerits. Authors in [8] have also proposed a HVDC subsea structure based on the modular conversion, also known as modular stacked direct current trans-

mission (MSDC). This structure employ various multilevel converter modules which are connected in series to achieve high voltage DC operation as shown in the Fig. 3. The sending and the receiving end converter modules are operated in current controlled mode, wherein the sending end converter voltage is varied to maintain the required current and supply the load. The subsea loads, located apart in this configuration, require large number of penetrators and wet-mate connectors, which are quite expensive and highly unreliable. As a result, reliability of the system becomes poor. Hence, there is still need for further study and development of reliable and cost effective subsea power transmission and distribution architectures.

III. Subsea Power Transmission and Distribution Systems

In this section a brief overview and limitations of various subsea power system components are highlighted.

A. High Voltage Power Umbilical

In subsea applications, the long distance high power and high voltage transmission/distribution require strong power cables with good insulation capability. The power umbilical can be fully electric or multiplexed wherein both electrical and hydraulic lines are combined. The cross sectional view of a typical multiplexed subsea power umbilical is shown in Fig. 4 [2]. Currently, advancements in the subsea umbilical technology allow manufacture of cable for both single and three cores with bulk power transfer capability. It is also possible to produce continuous umbilical cables of lengths up to 100 km. However, such long cables weigh in excess of 8000 tons and handling them is very difficult. This requires the manufacturing facility to have off-loading cable equipment at the site [13]. Apart from the design of subsea power umbilical, handling and maintenance also presents many challenges. The power umbilical must withstand several mechanical forces acting on it, such as force generated by its own weight, and the force due to the tidal currents. It may also be noted that, the subsea umbilical should survive due to various activities such as damage by anchors, fishing, vessel impact, and movement of the cable or seabed terrain. In general, to protect the umbilical from such events, one or two layers of metallic armor wires are provided during manufacturing.

The parametric model representation of the subsea cable in the subsea transmission differs completely from the conventional long distance transmission parametric models. Accurate model of the power umbilical is needed in order to study the effects of physical factors that come into picture in the subsea environments. The impedance will no longer be lumped, instead it will be a distributed parameter. In addition, the effects of skin and proximity phenomena become significant under such harsh environmental operations. Additionally, impedance of the power umbilical is highly frequency dependent due to the presence of large number of metallic parts within it. The subsea cable insulation coordination and its design have to consider all the above mentioned factors into account. As these cables are affected by various transient actions such as switching, sudden

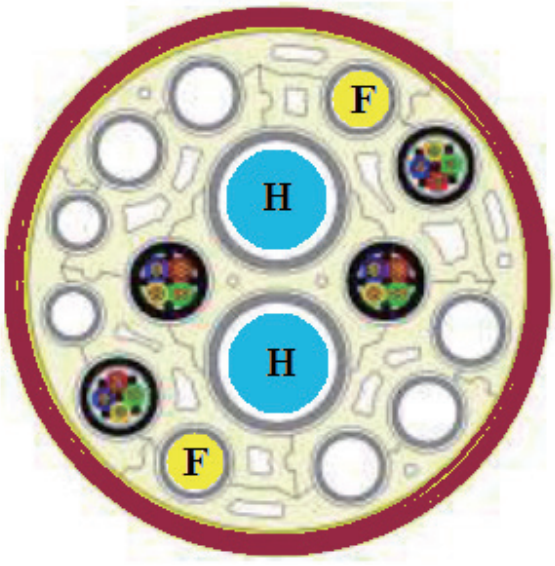

Fig. 4. Multiplexed electro-hydraulic subsea umbilical.

load change, and harmonic operation, a proper analysis for the electromagnetic transient behavioral study has to be conducted [20]. However, this study needs the exact model of the power umbilical, and it is very difficult to get the exact model. Some of the existing algorithms such as Bergeron's travelling wave model and frequency dependent model in phase domain are being considered in most of the studies.

B. High Voltage Switchgear

The HV switchgear for HVAC based subsea transmission and distribution system does not impose serious issues and challenges when compared to the HVDC transmission. The switchgear is usually kept within an enclosure and SF6 gas is used as an insulating media for providing isolation (3.3 kV to 36 kV) [21]. In subsea applications, reliability (more than 20 years) is the main design criteria and using a conventionally available switchgear make the system cost effective.

Advancements in the semiconductor industry and voltage source converters make the HVDC transmission with multi terminal grid possible. Main barrier for the use of HVDC transmission is the availability of switchgear. The impedance seen by the DC source is relatively low in comparison to the AC system, hence circuit breaker should react to the fault very quickly and isolate the fault. In addition, absence of current zero crossing in the DC system imposes several challenges in the design of HVDC breaker. In order to maintain the reliability of supply system, the fault should be cleared within a few milliseconds. In this regard, numerous HVDC circuit breaker (CB) designs have been reported in the literature [21], [22]-[25]. The HVDC CBs are classified into two categories namely, solid state CB and the hybrid CB. In solid state CBs, semiconductor devices are being used, which enables fast interruption capabilities. However, series resistance of the device at higher power levels results in significant amount of power losses. The power losses are minimized by using hybrid CBs, wherein an ultra-fast mechanical

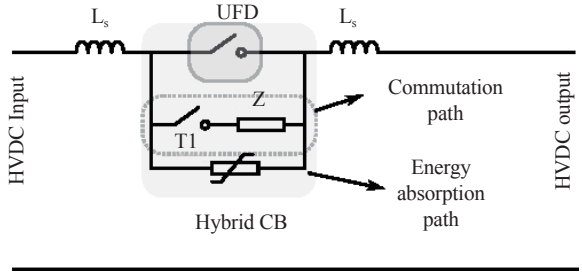

Fig. 5 Hybrid HVDC circuit breaker (Ls- refers to network inductance).

switch (UFD) in parallel with an artificial current zero crossing circuit is connected as shown in Fig. 5. Under normal condition, the load current is made to flow only through the UFD, and the parallel branch is activated only during the fault. A varistor in parallel with the HVDC CB is connected to discharge the energy stored in the network inductances. Use of varistors, especially for subsea applications, results in a large footprint. Hence, there is a scope for HVDC circuit breaker development with reduced footprint.

C. High Voltage Power Transformer

High voltage power transformers play an important role of step up/down of transmission and distribution voltages in the subsea power systems. Power rating of these subsea transformers may range from 500 kVA to several MVAs. The transformers are designed to operate in the frequency range of 25 Hz to 75 Hz. The subsea transformer must be designed to withstand the pressure levels imposed by sea water at depths of 3000 m. In addition, it should be able to operate well without maintenance for longer duration of the order > 25 years. Many leading electrical companies (ABB, SIEMENS, etc.) produce subsea transformers for high power ratings. These transformers are classified as single shell and double shell type. For pressure compensation, these transformers are filled with liquid which balances the pressure imposed by sea water with the internal pressure. A typical subsea transformer developed by SIEMENS, which is tested and qualified for 3000 m subsea operation is shown in Fig. 6 [26]. To maintain the reliability, it is required to continuously monitor the health of the transformer. It is also important to have an online diagnostic algorithm to identify and rectify the fault. There are many fault detection algorithms reported in the literature such as frequency response analysis (FRA), dissolved gas analysis (DGA), etc.

In HVDC subsea power transmission, DC power is converted to AC before connecting it to the load. The DC to AC conversion with present semiconductor industry enhancements can be performed in two different stages (DC-AC-AC). Initially, DC voltages are converted to high frequency (<1 kHz for high power) alternating voltages. Step up/down of the voltage is performed using a high frequency transformer and later it is fed to a high frequency AC to a line frequency AC converter. As this configuration employs a higher frequency transformer (solid state transformer) for the voltage transformation, footprint of the power system become smaller. However, these transformers

Fig. 6 Subsea power transformer (photo courtesy: SIEMENS).

have not yet made their impact in subsea applications.

D. High Voltage Wet-Mate Connectors and Penetrators

Wet-mate connectors and penetrators are the main limitations for the high voltage subsea power transmission. Currently, only AC wet-mate connectors are available up to voltage ratings of 36 kV with a maximum current rating of 500 A (MECON^{TM} WM-36) [27]. Similarly, AC penetrators have been reported up to a voltage of 60 kV with 630 A (SpecTRON-60) current rating, however the subsea depth for this penetrator is limited to 2000 m [28]. Penetrators and the wet-mate connectors are the weakest points in the entire subsea power system. Hence, reliability of the supply system greatly dominated by these components. In general, these components have a designed reliability of > 25 years under the sea.

For next generation efficient HVDC transmission and distribution of power in the subsea, wet-mate connectors and the penetrators are major barriers. Even today, subsea industry has not been able to develop these two components for the HVDC. Hence, development of HVDC wet-mate connectors and the penetrators can be considered as an evolution in the subsea industry.

IV. Power Electronics for Subsea Power Systems

The power electronics converter technology has been considered for several subsea and downhole applications. A few of the applications are:

- Electrical drives for oil well drilling
- Wireless power transfer between modules and to minimize the replacement of batteries
- Replacing the wet mate connectors by power electronic based converters particularly in subsea dc transmission system, deploying Solid state circuit breakers, etc.
- Powering the subsea electrical systems by offshore wind energy or by ocean energy such as under water current
- Power supplies for control and monitoring
- Power converters for electrically heating of subsea pipeline

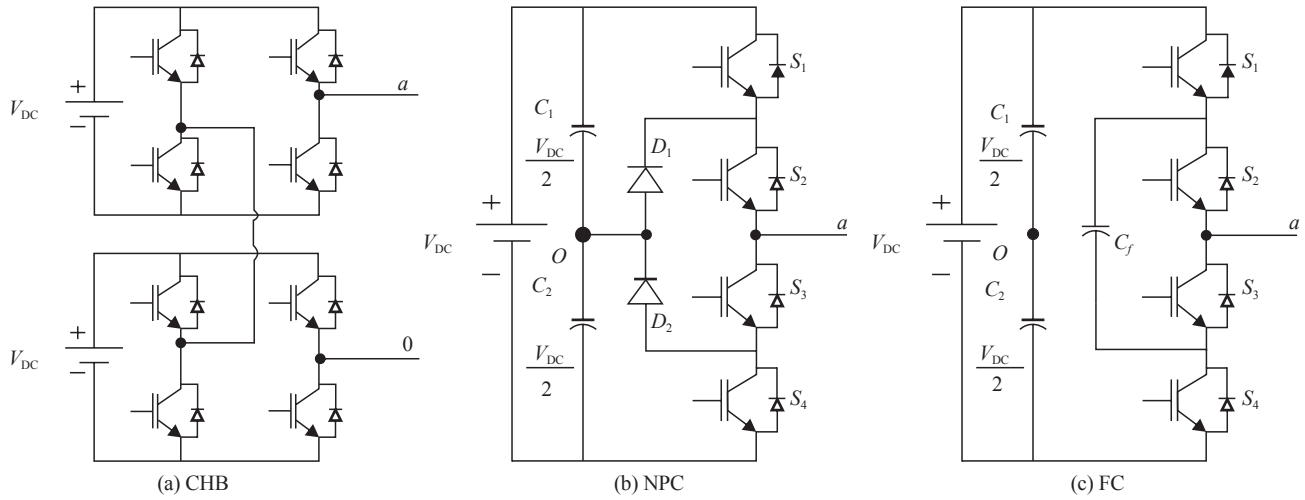

Fig. 7 Multilevel inverter topologies (one leg), (a) cascaded H-bridge, (b) neutral point clamped converter, (c) flying capacitor converter.

A variety of power electronic converters such as HVDC station converters, rectifiers, variable frequency drives (VFD), AC-AC converters, uninterrupted power supplies (UPS) and active front end converters, etc., are being employed in the subsea power transmission and distribution systems. This section provides an insight on the basic inverter topologies and their pressure tolerant operation in the subsea environments.

A. Power Converters or VFDs

Power converters are used for driving motors, which in turn connected to ESP and compressors that are used for boosting of oil and gas in the subsea. The power rating of the ESP and compressor systems together with the associated power converter is of the order of several MWs. Power converter or inverter is broadly classified as two-level and multilevel voltage source inverters. Two-level converters are being widely used in the industry, due to its simplicity. However, in high power and high voltage applications, the barrier for use of two–level inverter is the availability of high voltage rated devices. With the advent of multilevel inverters, it is possible to achieve high voltage operation with only existing low voltage rated devices. The conventional multilevel inverter topologies are broadly classified as neutral point clamped converters (NPC), flying capacitor (FC), and cascaded half bridge converter (CHB). The circuit diagrams of the popular multilevel converters are shown in the Fig. 7 [29]. The main limitation of these inverter topologies is that, they employ large number of components for achieving higher output voltage levels, thus affecting the reliability and increasing the complexity of the controller. These converters are being investigated for subsea power transmission and motor drives.

In modular multilevel converters (MMC), low voltage rated modules are cascaded to achieve high voltage operation. The MMC structures have a great fault tolerant capability, in terms of module failures. Faulty modules can be by-passed and system can still be operated normally but at reduced power or voltage levels. The possible application of MMC structures in the subsea HVDC transmission can be explored for future efficient subsea power architectures.

B. Pressure Tolerant Power Electronics and Vessels

As discussed in the previous sections, power electronic converters play an important role in the subsea applications. They need to operate at depths of up to 3000 m and at such water depth levels, pressure on the equipment may reach up to 300 bars. The power electronic converters are made to work at such conditions by enclosing them in pressure vessels that are filled with incompressible medium such as dielectric fluids. The dielectric fluid being a good insulator should also be able to have a good thermal conductivity in order to help the cooling of the power electronic system [11]. The essential properties of a dielectric fluid are high breakdown voltage, high temperature stability, nontoxicity, biodegradable, and good tolerance to moisture levels. The currently existing dielectric liquids are mineral oil, synthetic oil, silicon oil, and orgonic esters [11].

The main components of power converters are Insulated Gate Bipolar Transistor Devices (IGBT), DC link electrolytic capacitors, and the gate drivers, digital signal processor boards and sensors, which are mounted inside the pressure vessel. Existing configurations employ a one bar pressure chamber/vessel, in which the power converter is enclosed. However, for deep water applications with pressure levels of 300 bars and high power rating of several MWs, and the wall thickness and size increases. This reduces the thermal conductivity, wherein the heat generated from the converter does not flow to the sea water effectively, resulting in poor cooling of the converter. To address the above listed issues, recently SINTEF has proposed a new concept wherein the vessel is designed for 300 bar pressure with reduced wall thickness [10], [11]. In addition, component level pressurization is being tested for power components such as IGBTs, electrolytic capacitors, and the gate drivers. Various sealing and packaging methods for two IGBT technologies, bonded IGBT and press-pack IGBTs, with the experimental test

validation are reported in [11].

V. Health Analytics and Fault Handling

With the price of oil per barrel reaching its lowest value in a decade during early 2016, the industry started taking significant steps to reduce the cost of production. A major initiative has been to improve the reliability of equipment and identify fault scenarios at an earlier stage itself so that the high costs associated with failed equipment and down-time can be reduced. This has led to increased focus on predictive fault evaluation and system health analytics for subsea and sub-surface equipment, including power converters.

Traditionally, reliability predictions have been done according to different handbook models and terms, such as mean time to failure (MTTF) and mean time between failures (MTBF). But these evaluations only consider constant failure rate and usually disregard effects due to wear out. Recently, some research findings were reported to identify more accurate methodologies for power converter reliability predictions via physics-of-failure and mission profile analysis [30]. It is important to consider the actual mission profile for power converters to more accurately predict the reliability. Moreover, with various statistical tools available at present [31], it is possible to continuously assess the health of power converters real-time using recent data from sensors and take judicious decisions. If a fault scenario is predicted, it will also be possible to complete a task at a lower system stress level and fix the equipment at the next possible opportunity, thereby reducing the chance of an unscheduled repair that can cost millions of dollars to the operators. Though such analysis have been performed in power converters for renewable energy (such as wind, solar, etc.), hardly any research activities have been reported in fossil energy industry. The extreme environments of temperature, pressure, vibrations, etc. faced by power converters in oil and gas industry make it hard and challenging to perform an accurate reliability study, since the components in such systems are many a time operated at the edge of their physical capabilities. This will require mission profile modeling of extreme environments and failure analysis of components using highly accelerated stress testing (HASS) and/or highly accelerated life testing (HALT). These tests will provide information on the type of failure, example device breakdown, bond rupture, thermal runaway, etc. It is time to perform extreme environment reliability predictions and analytics to monitor real-time system health monitoring and diagnostics.

Another important research area is to arrive at effective fault tolerant power conversion systems including reconfiguration, redundancy, etc. thereby the system can continue to operate at a lower stress level until a task gets completed. Evaluating alternate converter strategies, such as Z-source inverter based motor drives for ESPs, can also add significant value.

VI. Conclusions

This paper presented the main requirements and challenges of using electrical components and power electronics systems, and adapting suitable system architectures in subsea environment. Various existing HVAC and HVDC subsea power architectures with their merits and demerits were discussed. This paper also addressed the critical parameters to be considered, and the required components for the future efficient and cost effective HVDC transmission and distribution systems. Various opportunities for advancement and development for electrical systems in the subsea power industry are:

- High power density power conversion systems
- Fast acting solid state circuit breakers with galvanic isolation capability
- Wet-mate connectors for high voltages
- Penetrators for high voltage systems
- Fault and pressure tolerant power electronic converters
- Health analytics and diagnostic systems

The above listed requirements and challenges for subsea applications present a wide range of opportunities for research and improvements, thus leading to efficient and more environmental-friendly subsea oil recovery system.

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Review on Distributed Energy Storage Systems for Utility Applications

Liuchen Chang, Wenping Zhang, Shuang Xu, and Katelin Spence

***Abstract*—Energy storage systems (ESSs) can improve the grid's power quality, flexibility and reliability by providing grid support functions. This paper presents a review of distributed ESSs for utility applications. First, a review of the energy storage market and technology is presented, where different energy storage systems are detailed and assessed. Then, ESS grid support functions are presented and seven types of functions are described. Finally, the power electronic converters for distributed ESSs are reviewed and the corresponding features and performances are evaluated. The main objective of this paper is to provide an updated reference regarding ESSs for utility applications to researchers and practitioners in the field of power electronics.**

***Index Terms*—Energy storage systems, grid support functions, power conversions.**

I. Introduction

CLIMATE change and global warming pose a threat to our environment and health and are growing in significance due to the increase of greenhouse gas emissions [1]-[2]. Renewable energy resources (e.g. wind and photovoltaic etc.) are gaining attention due to their low emissions and abundance. However, the intermittent nature of renewable resources like wind and solar energy also brings new issues regarding the grid's reliability, flexibility and power quality. Therefore, energy storage systems (ESSs) are being introduced to address these issues. Smart grid technologies make it possible to reduce and shift loads and support renewables [3]-[4]. The ESSs in a smart grid are able to improve grid reliability, flexibility and power quality by providing grid support functions such as ancillary services and peak load reduction [5].

Based on energy storage technologies, ESSs can be divided into five categories: electrochemical, electromagnetic, mechanical, chemical, and thermal [1]-[4]. Each storage system has distinctive characteristics in terms of power rating, discharge time, power and energy density, response time, self-discharge losses, life and cycle time, etc. , [6]-[9]. These features should be taken into account to determine their suitability for different grid support functions, such as peak shaving, energy arbitrage, integration of renewables, voltage and frequency regulation, harmonics compensation, spinning and non-spinning reserves, and black start [15]-[20]. In order to fulfill these functions, power electronic conversion technologies are critical in controlling the power flow between the grid and ESSs. Two power conversion structures, common DC bus and AC bus, are normally applied. In addition, various bidirectional converters (DC/DC, DC/AC, and AC/AC) are employed to improve the system performance. System performance can pertain to efficiency, reliability, output distortion and power density.

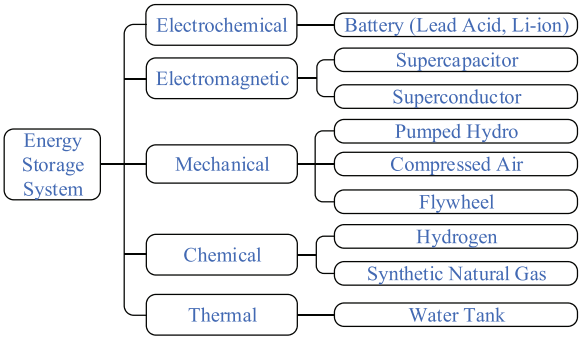

Fig. 1. ESS classifications.

The objective of this paper is to review ESS technologies, grid support functions and power converters for ESSs. In this paper, Section II presents a review of the energy storage market and technology, where different energy storage systems are detailed and assessed. Section III presents the ESS grid support functions and seven types of functions are described. In Section IV, the power electronic converters for ESSs are reviewed and the corresponding features and performances are evaluated. Section V concludes this paper by remarking on future trends in these areas.

II. Energy Storage Technology

The five categories of ESSs are presented in Fig. 1 [1].

The market of ESSs for utility applications has been developing rapidly as presented in Fig. 2, where the market is still dominated by pumped hydro storage (PHS) systems [2]. With the technological development, new forms of ESSs, such as electrochemical ESSs, have grown significantly.

A. Energy Storage Technologies

1) Electrochemical ESS

Electrochemical ESSs are generally referred to as batteries. A traditional battery is lead acid (LA). LA batteries have

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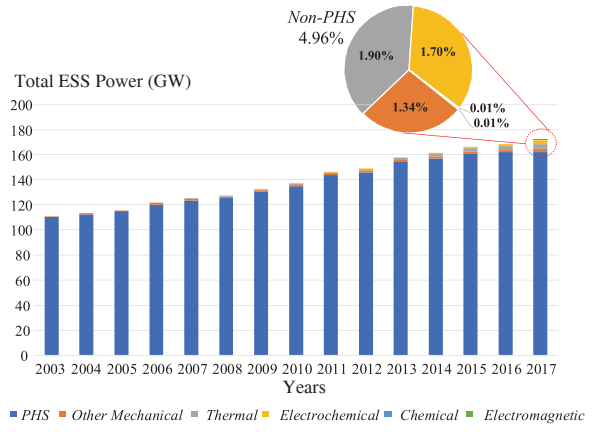


Fig. 2. Global power capacity of ESS.

been widely applied due to their well-developed technology and low costs. However, the disadvantages, such as limited cycle lifetime, low energy density and environmental impact, will limit their application in the future [3].

On the contrary, lithium ion (Li-ion) batteries have higher power and energy density, higher number of lifetime cycles, and higher efficiency, which are promising for grid applications [1]. However, the safety risk is still a challenge because of their flammable electrolytes. Additionally, the Li-ion battery costs are relatively high.

Recently, some research has focused on flow batteries, such as vanadium redox batteries (VRBs). VRBs feature extremely long lifespan and lifetime cycles with power up to several MW [4]. However, the main drawback is that the efficiency of VRBs drops significantly in cold temperatures, which narrows its application.

2) Electromagnetic ESS

Electromagnetic ESSs can store energy in either electric fields (e.g. supercapacitors) or magnetic fields (e.g. superconductors). Compared with batteries, supercapacitors have higher reliability, lower maintenance, and lower environmental impact [5]. However, low energy density makes supercapacitors unsuitable for long-term discharging applications.

Superconducting magnetic energy storage (SMES) features fast dynamic responses. Theoretically, the energy in SMES can be stored forever due to zero losses of superconducting materials [6]. However, there is a strict requirement of maintaining a low temperature for the SMES to operate and the corresponding costs limit its applications.

3) Mechanical ESS

Mechanical ESSs transform energy between mechanical and electrical forms. Surplus electricity is taken from the grid during off-peak hours and stored mechanically (by gravitational potential or rotational energy) until it is needed; it is then released back to the grid [7].

The most common system is pumped hydro, which has a high power and energy rating, long lifespan, and practically unlimited life cycles. However, the dynamic response is slower than some other ESSs. PHS also has a large geographical footprint and specific topographical requirements.

Compressed air energy storage (CAES) systems store energy in the form of intermolecular potential energy. It features a large capacity and medium geographical dependency. However, the round-trip efficiency is low because of heat dissipation [8].

Compared with other mechanical ESSs, flywheel energy storage (FES) systems have the highest power density and lowest geographical dependency. However, the primary disadvantage is that the friction between rotor and shaft affects the system efficiency, in addition to the high costs.

4) Chemical ESS

Typical chemical ESSs are hydrogen ESS and synthetic natural gas (SNG) ESS. A hydrogen ESS decomposes water (H_2O) into hydrogen (H_2) and oxygen (O_2) with electricity. Then, H_2 can be stored in high-pressure tanks and fed into a fuel cell to produce electricity. This is an effective way of storing a large amount of energy for a long period, which can be applied for long term or even seasonal applications [9]. However, the main limitations are the high costs for obtaining hydrogen and full cell equipment and the safety risk of storing pressurized H_2.

Another method of long term electricity storage uses SNG. For the same amount of energy storage, the pressure of a SNG tank is lower due to the higher density of SNG. However, compared with hydrogen ESS, the conversion losses of SNG ESS are higher and the round-trip efficiency is lower [10].

5) Thermal ESS

Water storage tanks can be adapted for use as thermal ESSs. They work for load shifting functions, where the temperature of a water tank is raised during off-peak hours so that hot water and warm air can be provided during peak hours without drawing as much electricity. However, this scenario is essentially load control and the regulation capability is inflexible, especially during summer months or in hot regions where limited hot water or heat is needed [11].

B. ESS Comparison

Different ESSs are compared in the following in terms of power density, energy density, power capacity, discharge time, cycling times, and efficiency etc.

1) Power & Energy Density [1]-[4]

Fig. 3 presents the power and energy density ranges of different ESSs in terms of power or energy per liter.

Based on Fig. 3, it can be seen that most batteries and flywheels have relatively moderate energy and power densities. Comparatively, Li-ion batteries have higher energy and power densities than LA batteries. Also, the energy density of the VRB flow batteries is low. Mechanical ESSs (PHS and CAES) have low power and energy densities, since large reservoirs are required. Supercapacitors have high power densities but low energy densities and in comparison, SMESs have a lower power density. The energy densities of the hydrogen and SNG ESSs are relatively high.

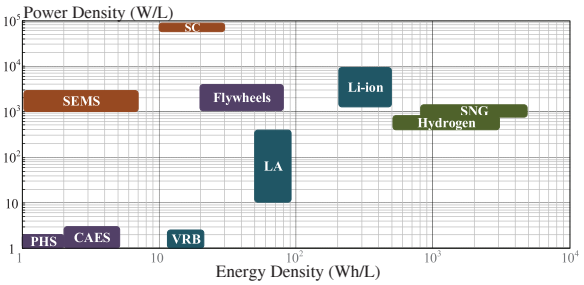


Fig. 3. Power and energy density comparison for ESSs.

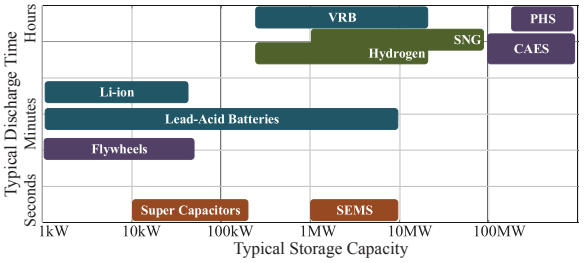


Fig. 4. Typical power capacity and discharge time for ESSs.

2) Power Capacity and Discharge Time [4]-[11]

Based on Fig. 4, it can be seen that electromagnetic ESSs, such as SC and SMES, have short discharge times of several seconds. This makes them useful for short-term grid support functions. On the contrary, mechanical and chemical ESSs have long discharge times in the range of hours, which can be applied for long-term functions such as load shifting. The PHS and CAES mechanical ESSs are suitable for high-power applications, as are the hydrogen and SNG chemical ESSs. Electrochemical and electromagnetic ESSs generally have a lower power capacity, but their applications in the distributed energy systems secure them a decent market share.

3) Additional Features [5]-[9]

Additional technical characteristics are presented in TABLE I. It can be seen that batteries, SC and SMES all have fast response times. Mechanical ESSs, including PHS, CAES and flywheels, have higher cycling times. Additionally, PHS, CAES and hydrogen ESSs have very small daily self-discharge ratios, which means the energy can be stored for a long time.

III. ESS Grid Support Functions

Based on response time, grid support functions can be divided into three categories: second-level, minute-level and hour-level, as presented in Fig. 5 [12]. In order to be useful for grid support functions, ESSs are required to have the both fast power response and high energy capacity.

A. Peak Shaving & Load Leveling

As shown in Fig. 6(a), if the load demand P_{Load} is higher than the maximum scheduled generation P_{S_max}, ESSs can discharge power to shave the peak load. If the load demand

TABLE I
Additional Technical Characteristics

	Daily Self-Disc (%)	Lifetime (years)	Cycling Times (cycles)	Discharge Efficiency (%)	Response Time
LA	0.1–0.3	3	~1000	~85	milliseconds
Li-ion	0.1–0.3	5–10	~5000	~85	milliseconds
VRB	Small	5–15	~10000	~85	milliseconds
PHS	~0	40–60	~30000	~87	minutes
CAES	~0	20–40	~10000	~75	minutes
FES	100	~15	~20000	~90	seconds
SC	20–40	10–30	~50000	~95	milliseconds
SMES	10–15	20+	~100000	~95	milliseconds
H_2	~0	15	~10000	~59	seconds
SNG	~0	15	~20000	~50	seconds

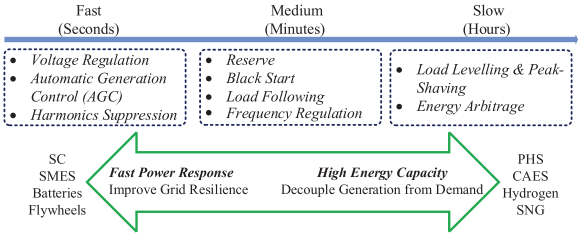


Fig. 5. Grid support function diagram.

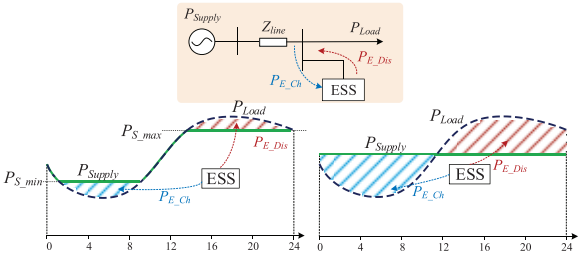


Fig. 6. Peak shaving & load leveling function.

P_{Load} is lower than the minimum scheduled generation P_{S_min}, ESSs can store the excess energy. Load leveling is similar to peak shaving, as shown in Fig. 6(b). The difference is that peak shaving is focused on flatting the load peak, while load leveling attempts to flatten the entire load [13]. These functions can reduce fuel consumptions and carbon dioxide (CO_2) emissions, decrease maintenance costs, and increase system reliability. Research related to this focuses on four aspects:

1) Obtaining the optimum charging & discharging schedule for ESSs;
2) Finding the optimum size and placement for ESSs;
3) Assessing economic costs for customers and utilities and improving the economic feasibility;
4) Implementing distributed ESSs instead of large-scale ESSs.

Recently, research has also focused on the use of electric vehicles (EVs) for peak-shaving. However, the main challenges are the availability of EVs, aggregated control of large-scale EVs, and the corresponding infrastructure for EV inte-

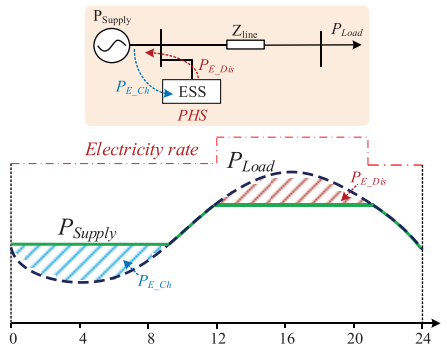


Fig. 7. Energy arbitrage function.

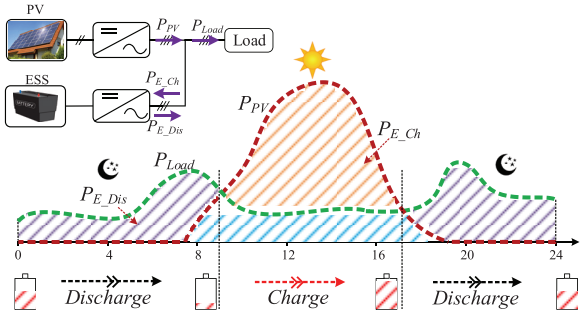


Fig. 8. Integration of PV systems.

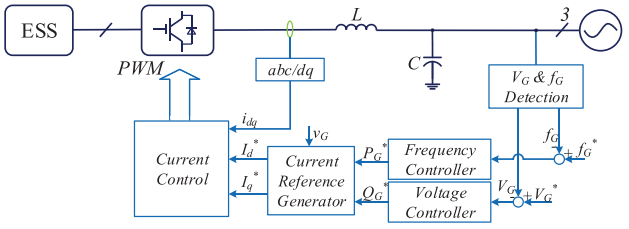


Fig. 9. Voltage & frequency regulation control diagram.

gration with the grid.

B. Energy Arbitrage

Energy arbitrage is attempting to earn a profit by charging the ESS at a lower electricity rate and selling the stored energy at a higher price, which is presented in Fig. 7 [13]. Traditionally, this function is implemented by pumped hydro storage (PHS) systems. With the wide application of EVs, numerous charging scheduling are proposed for energy arbitrage. The large quantity of EVs in the near future could contribute to a new concept of the energy market.

Energy arbitrage research is similar to peak-shaving functions; which includes the optimum ESS scheduling for maximizing the profits, ESS sizing, economic assessment, and implementation of distributed ESSs, especially EVs.

C. Integration of Renewables

The intermittent nature of renewable energy sources introduces new challenges for power system operation. The main

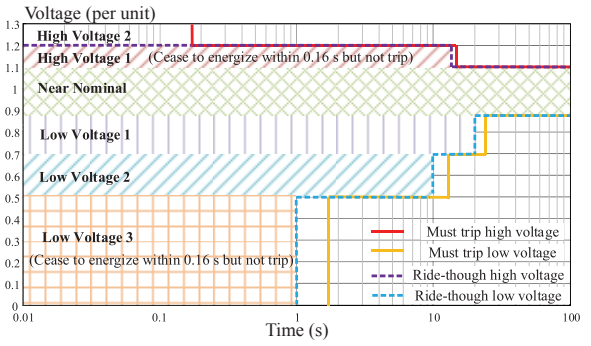


Fig. 10. Voltage ride-through requirements.

issue is the unpredictable power imbalance between generation and demand [14]-[15]. Therefore, ESSs are introduced to balance the intermittency. In addition, ESSs can be used to smooth out fast load fluctuations, regulate frequency, etc. Integration of renewables requires more system resources to provide ancillary services (seconds and minute-levels) and energy dispatch (hour-level). While this topic covers a wide scope, only longer term energy storage is described here. Fig. 8 presents the basic concept of ESSs supporting PV integration for load balancing. The ESSs are charged in the daytime, when PVs generate power, and are discharged at night when PV power is unavailable. As a result, the system power is balanced and the reliability is enhanced. There are four research topics related to this:

1) Finding optimum system integration configurations;
2) Mathematically modelling intermittency for renewable energy sources;
3) Selecting ESS type, size, and siting to optimize cost;
4) Designing control structure and scheduling strategies for energy flow management.

D. Voltage & Frequency Regulation

ESSs can be used to absorb real power when the grid frequency is higher than nominal and inject real power when the grid frequency drops below nominal [16]-[17]. By doing this, they help to stabilize the grid's frequency. Similarly, ESS can contribute to voltage regulation by injecting or absorbing reactive power. The control diagram is presented in Fig. 9. SCs, FESs, and batteries are normally adopted for frequency and voltage regulation because of their fast response.

UL 1741 specifies the voltage and frequency ride-through requirements for distributed energy resources (DERs), which are shown in Fig. 10 and Fig. 11.

E. Harmonic Compensation

Due to the increasing presence of nonlinear loads and power electronic converters, the grid power quality is deteriorated significantly. To compensate grid harmonics, numerous active and passive filtering techniques were developed [18]-[19]. However, installing additional filters is not favorable due to extra costs. An alternative is utilizing ESSs to compensate harmonics where harmonic compensation can

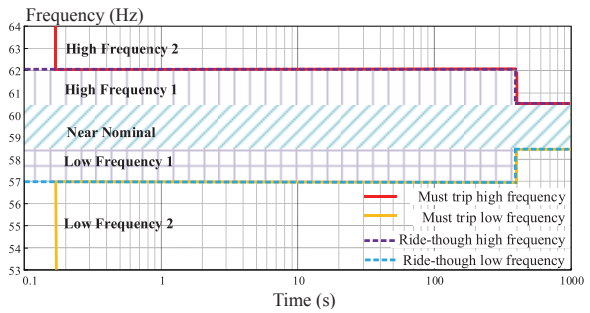


Fig. 11. Frequency-ride through requirements.

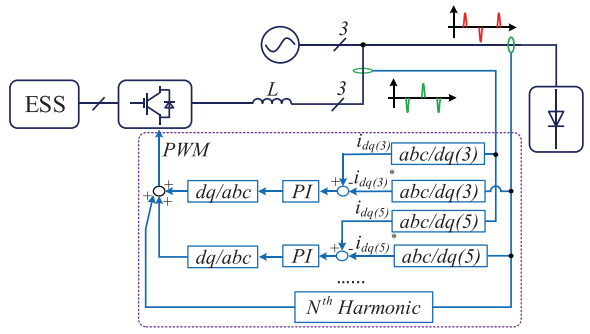


Fig. 12. Harmonics compensation control diagram.

TABLE II
MAXIMUM HARMONIC CURRENT DISTORTION

Harmonic Order h	h<11	11≤h<17	17≤h<23	23≤h<35	h≥35	Total Demand Distortion
Percent (%)	4.0	2.0	1.5	0.6	0.3	5.0

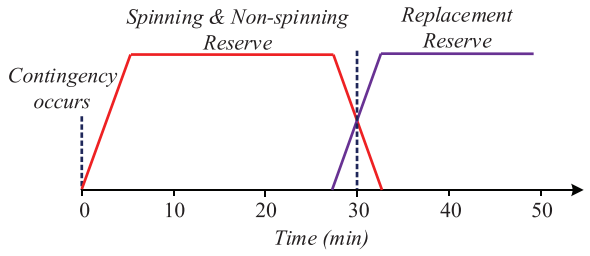


Fig. 13. Different reserves respond to a contingency.

be integrated with primary grid support functions. Fig. 12 presents a harmonic compensation control diagram, where the 3rd and 5th harmonics are transformed into corresponding *d-q* coordinates for current harmonic suppression.

IEEE 1547 specifies the maximum harmonic current distortion for DERs, as shown in TABLE II.

F. Reserves

When a contingency occurs and is large enough to affect the power system frequency, the spinning reserves instantly respond as shown in Fig. 13 [20]. Then, the spinning and non-spinning reserves are normally relieved by replacement reserves within 30 minutes. Therefore, the reserves are an important resource that can safeguard power systems without involuntary load shedding. Currently, battery storage systems are being gradually applied for spinning reserve to replace conventional generators which are slow for grid synchronization due to startup issues.

Increasing the grid reserve size can increase the system reliability, but with higher costs. Numerous approaches have been proposed to determine the optimum spinning reserve size as a compromise between reliability and costs. Currently, with the increasing penetration of EVs, some research is also conducted on evaluating the spinning reserve ability of EVs.

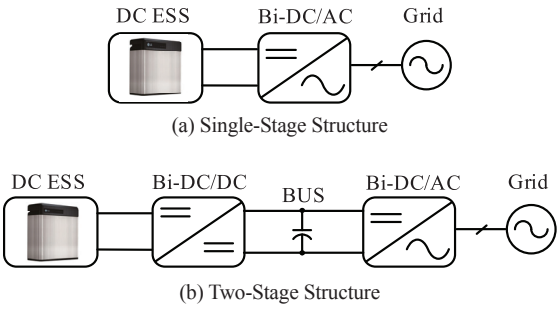


Fig. 14. DC ESS structure.

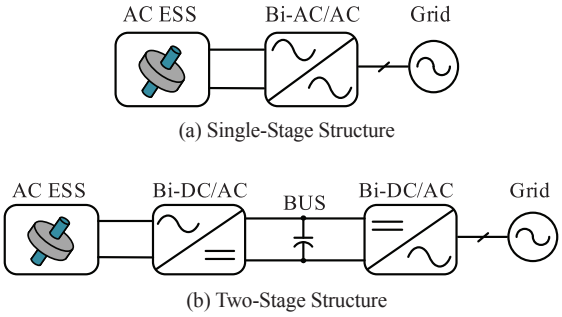


Fig. 15. AC ESS structure.

G. Black Start and Load Following

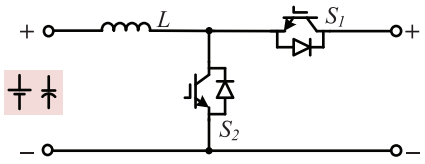
ESSs can provide black start capability, which helps a system startup from a shutdown. An example is the *Huntorf* CAES plant that provides black-start power to nuclear units located near to the North Sea [5], [21].

Also, ESSs can provide support for following the load demand changes. Some relevant research and demonstration projects can be found in [5] and [22].

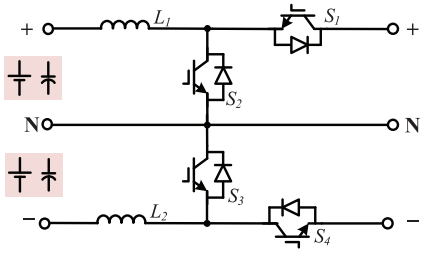
IV. ESS POWER CONVERTER TECHNOLOGY

Typical distributed ESSs are batteries, supercapacitors, SMESs and flywheels. These ESSs can be categorized as DC ESSs (e.g. batteries) and AC ESSs (e.g. flywheels). Fig. 14 and Fig. 15 present the typical structures for DC ESSs and AC ESSs respectively; including single-stage and two-stage structures.

From Fig. 14 and Fig. 15, typical power converters for



(a) Single Buck/Boost



(b) Series-Output Dual Buck/Boost

Fig. 16. Bidirectional buck/boost converter.

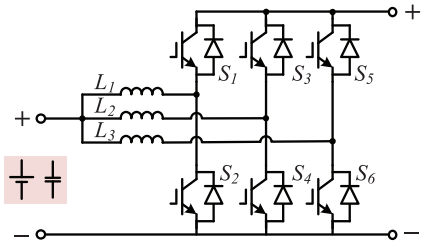


Fig. 17. Bidirectional interleaved DC-DC converter.

ESSs include bidirectional DC/DC, bidirectional DC/AC, and bidirectional AC/AC. In general, power converters should have the following features:

1) Bidirectional power flow;
2) High efficiency.

In addition to these features, for different applications:

3) Fast response (e.g. frequency regulation applications);
4) High peak power (e.g. peak shaving applications).

A. Bidirectional DC/DC Converters (Bi-DC/DC)

A typical non-isolated Bi-DC/DC structure is the buck/boost converter, which is presented in Fig. 16 [23]-[24]. Compared to Fig. 16(a), the topology in Fig. 16(b) can be used for the applications where access to the DC bus neutral-point is needed. The buck-boost converter has a low number of power electronic devices, which leads to lower costs and higher reliability than other converters. However, it cannot be used in applications where isolation is required. Its voltage step-up ratio is relatively low, making it unsuitable for low-voltage ESSs. Additionally, the input current ripple is relatively high, which may be harmful for some energy storage, such as batteries.

In order to suppress the current ripple of buck/boost converters, interleaved topologies are widely applied. Fig. 17 presents the interleaved buck/boost converter. In addition to suppressing the ripple, a higher power rating can be achieved with the interleaved technology. However, the number of switches is increased which results in higher costs.

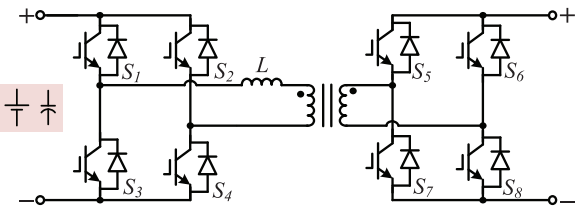


Fig. 18. Bidirectional dual active bridge DC-DC converter.

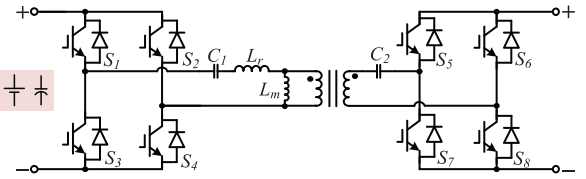


Fig. 19. *CLLC* DC/DC converter.

When isolation is required, dual active bridge (DAB) DC/DC converters are commonly selected as shown in Fig. 18. The output power can be easily regulated and zero voltage switching (ZVS) can be achieved [25]-[26]. However, compared with the non-isolated converter in Fig. 16, there are more power electronic devices, which reduces the system reliability. Furthermore, the conduction losses and turn-off loss are higher.

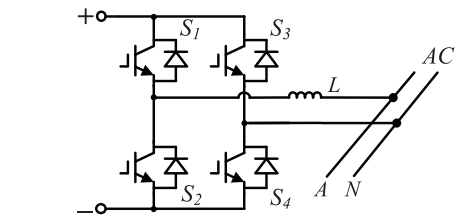
To improve the efficiency of DAB converters, numerous modifications, such as *LC*, *LCL*, and *CLLC* converters, are proposed [27]-[28]. Fig. 19 presents the *CLLC* DC/DC converter. The proposed topologies have higher efficiency but are more complex. Also, the output power regulation capability is limited due to soft switching.

B. Bidirectional DC/AC Converters (Bi-DC/AC)

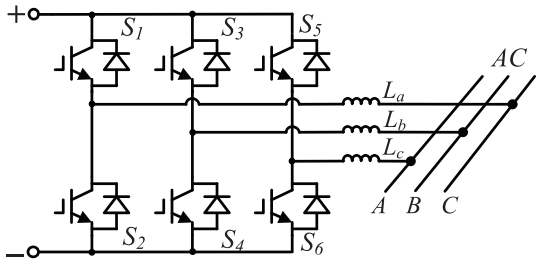
Currently, the most widely used DC-AC converters are two-level inverters as shown in Fig. 20, which can be single-phase and three-phase [29]. The bidirectional two-level DC-AC inverter has a compact design and high reliability. However, the switches experience higher voltage stress and the system efficiency is relatively low. Also, the output distortion is higher than multilevel inverters.

Multilevel DC/AC converters, such as the neutral point clamped (NPC) shown in Fig. 21(a), are introduced to improve the system efficiency [30]. Recently, the T-type topology, as shown in Fig. 21(b), has been widely used due to its higher efficiency and higher reliability. However, the neutral point voltage balance is still a key issue for three-level converters.

Operating with DC currents, SMESs require current source inverters (CSIs) [31], shown in Fig. 22. The dead time for the device gate controls is not required for CSIs. It is worth mentioning that the coils in SMESs are not allowed to be open, thus a bypass switch is normally paralleled with the coil during the standby mode. In addition, a leakage current occurs in CSIs due to the common mode voltage. Therefore,

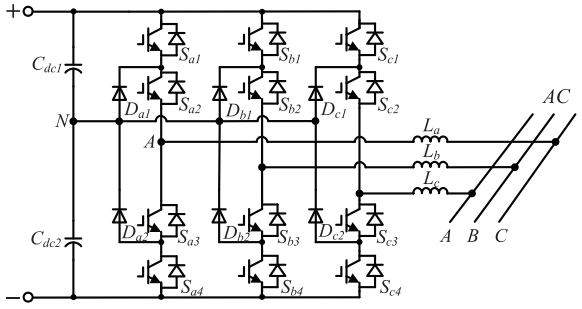


(a) Single-Phase

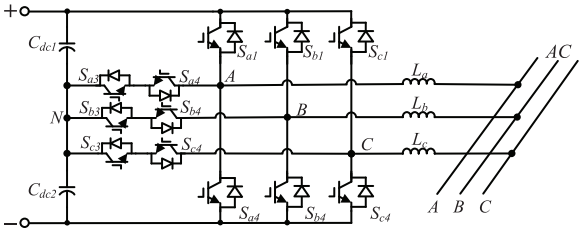


(b) Three-Phase

Fig. 20. Bidirectional two-level DC-AC converter.



(a) Neutral Point Clamped



(b) T-Type

Fig. 21. Neutral point clamped multilevel DC-AC converter.

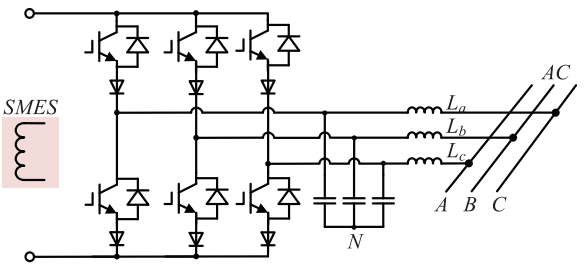


Fig. 22. Three-phase current source inverter.

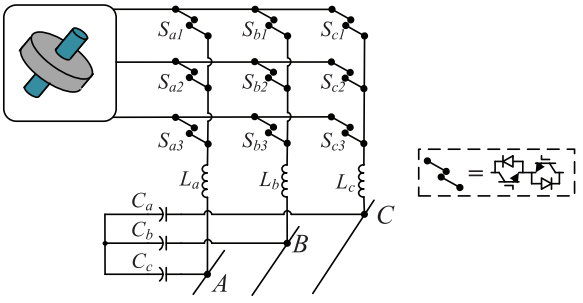
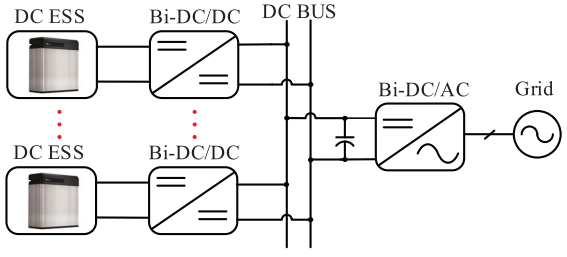
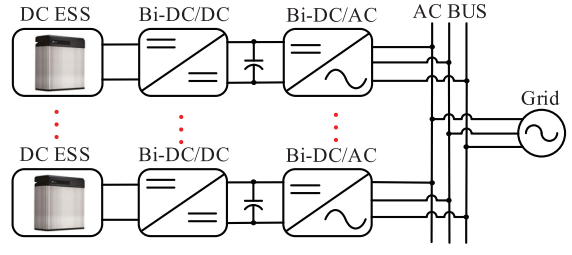


Fig. 23. Matrix AC-AC converter.



(a) Parallel DC Bus



(b) Parallel AC Bus

Fig. 24. Parallel DC and AC bus structures.

more topology modifications and modulation techniques have been developed to improve the performance of CSIs.

C. Bidirectional AC/AC Converters (Bi-AC/AC)

A typical AC-AC converter is the matrix converter, which is presented in Fig. 23. The matrix converter eliminates the DC-link, which has its merits. However, more bi-directional switches are involved, which makes the system more complex and costly [32].

ESSs are commonly combined to achieve a high power rating, large scale or high reliability for utility applications. Furthermore, parallel DC and AC busses are adopted for multi-ESSs applications, which is shown in Fig. 24. It is worth mentioning that for the parallel DC bus structure in Fig. 24(a), the reliability of DC/AC converter is critical; since all energy storage modules feed into one inverter.

Additionally, series DC or AC bus configurations are widely adopted for large-scale ESS applications. Fig. 25 presents a series DC bus structure [33], where high DC bus voltage and galvanic isolation can be achieved. This topology is suitable for DC inputs with low voltages or large variations. However, there is a decrease in efficiency when large voltage variations happen.

Modular multilevel cascaded (MMC) converters are one of

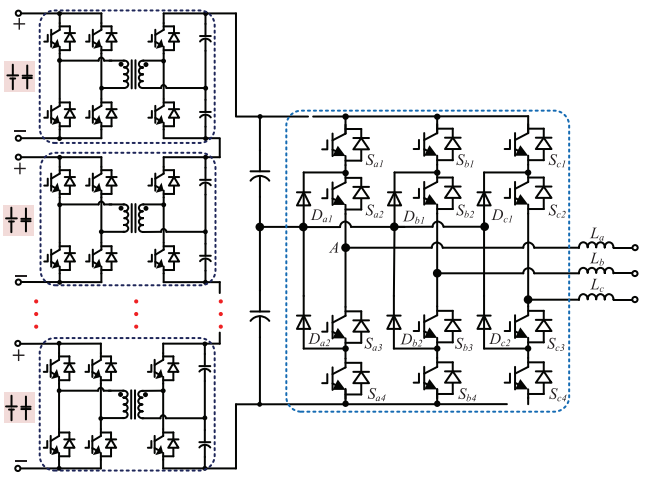
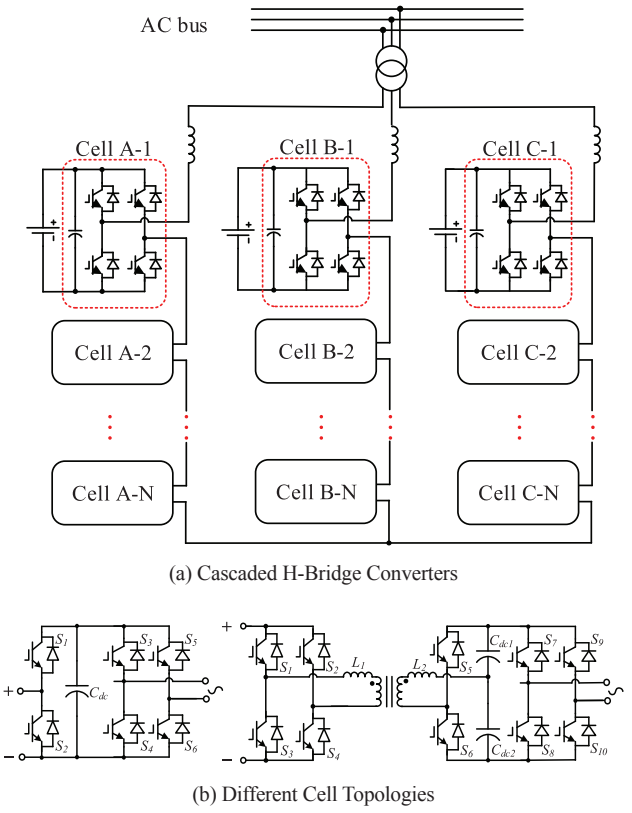


Fig. 25. Series DC bus configuration.



(a) Cascaded H-Bridge Converters

(b) Different Cell Topologies

Fig. 26. Series AC bus configuration.

the typical series AC bus structures, shown in Fig. 26(a). This topology features higher efficiency, lower output harmonics, and higher fault-tolerance; which is applied for large-scale battery ESSs [34]. Each bridge cell can dependently control the state of charge (SOC) of a battery. However, the additional hardware and software for balancing among different modules is still a main drawback. Instead of using H-bridge converters, the bridge cells can adopt other topologies for different applications. Fig. 26(b) presents two types of cell topologies.

V. Conclusions

This paper gives an overview of recent developments in ESS technologies. While there are various ESSs in the utility market, the continued development of low-cost and high-performance solutions is the main direction. Newly emerging ESS technologies need intensive investigation to gain utility acceptance in future. The factor of environmental friendliness will play a more and more important role for the fates of different ESSs.

No single storage type can satisfy all the utility requirements, therefore the selection of energy storage technologies is a key issue. Adopting hybrid ESSs, which can achieve multi-facet objectives, is a growing trend.

It is critical to optimize the design of ESSs in utility application by determining the size (e.g. power and energy capacity) and site of the ESSs. Various optimization methodologies, which consider costs, reliability and post-compensation performance indicators, have been proposed for ESS applications and will continue to be developed. Current power dispatch and scheduling for most ESSs are for ideal conditions. In the future various uncertainty factors, including renewable forecast error, technical constraints, and market rules, should be taken into account. Seeking a more robust optimization scheduling is at the forefront for research in utility operation.

The objective for power converter developments is to achieve high power, high efficiency, high reliability, and high power quality. For DC/AC converters, multilevel topologies are still dominant in the market high power units with higher efficiency and lower harmonic distortion; and two-level topologies are mainly for low power units. With increasing renewable energy penetration, the reliability of power electronic converters has become critically important.

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A Review of Envelope Tracking Power Supply for Mobile Communication Systems

Xinbo Ruan, Yazhou Wang, and Qian Jin

***Abstract*—In modern mobile communication systems, spectral efficient modulation formats have been widely used, which results in the envelope of the radio frequency (RF) signal is variable and having large peak to average power ratio (PAPR). In order to amplify the RF signal without distortion, the linear power amplifier (LPA) is adopted, which is less efficient when powered by constant voltage. Three popular techniques, i.e., Doherty, envelope elimination and restoration (EER), and envelope tracking (ET) techniques, to greatly improve the efficiency of the power amplifiers are analyzed and compared in this paper, and it is shown that the ET technique is the most suitable for future mobile communication systems. In the ET systems, the ET power supply is the key equipment, which dominates the system efficiency. With the development of the mobile communication systems, the bandwidth and the PAPR of the envelope signals are increasing rapidly, which pose severe challenges on the design of the ET power supply. This paper summarizes and sorts the ET power supplies in the literatures, and a detailed comparison is presented to guide the selection of ET power supplies for different applications. Finally, the methods, including soft-switching, slow envelope, and band separation are proposed for further increasing the efficiency of the ET power supply.**

***Index Terms*—Band separation, Doherty, envelope elimination and restoration, envelope tracking, power amplifier, slow envelope, supply modulator, soft-switching.**

I. Introduction

THE mobile communication brings convenience of real-time communicating to people in a mobile state without physical transmission line, and it has been continuously developing ever since its advent in 1970s [1]. The first-generation (1G) mobile communication systems adopted analog electronics technology and can only provide voice service. Furthermore, it suffered poor anti-interference ability and slow data transmission rate. The second-generation (2G) mobile communication systems employed digital electronics technology, and they can transmit and receive voice and text message. With the rapidly increased customers and the demand for multi-media service, the data transmission rate is required to be faster, and the third-generation (3G) and fourth-generation (4G) mobile communication systems emerged in succession, which makes the video calling service and internet surfing into reality [1].

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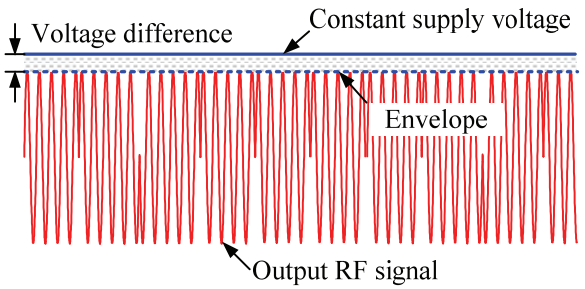

Fig. 1. Key waveforms of the LPA in 2G mobile communication system.

With the development of mobile communication, the power consumption increases rapidly, accounting for about 10% of the global power generation. Thus, it is necessary to reduce the power consumption of the mobile communication. In mobile communication systems, the base stations consume the majority of the power. In a base station, about 50% of the power is consumed by the power amplifier, and its loss is dissipated as heat, which requires extra power to cool down. So, increasing the efficiency of the power amplifier is the basis of reducing the overall power consumption of the mobile communication.

In 2G mobile communication systems, the modulation formats like Gaussian minimum shift keying (GMSK) and frequency shift keying (FSK) are employed [2]. Such modulation formats only modulate the phase and frequency of the radio frequency (RF) signal, and the amplitude of the RF signal does not carry any information. Thus, the envelope of the RF signal is constant, as shown in Fig. 1. Such signals can be amplified with nonlinear power amplifier (NLPA) or linear power amplifier (LPA). When LPA is adopted, the voltage difference between the supply voltage and the output RF signal of the LPA can be very small, as shown in Fig. 1, and the LPA can achieve relatively high efficiency [3].

In 3G and 4G mobile communication systems, for the purpose of accelerating the data transmission rate and making the most of the crowded and limited spectral resource, some spectral efficient modulation formats, such as quadrature phase shift keying (QPSK) and quadrature amplitude modulation (QAM) [2], have been adopted. In these modulation formats, the amplitude of the RF signal is modulated, and the envelope of the RF signal is no longer constant and it is variable with large peak-to-average power ratio (PAPR), as shown in Fig. 2. In order to satisfy the stringent linearity requirement of the output RF signal, LPA is usually employed. If the LPA is powered by a constant supply voltage, it would suffer from very low efficiency since the voltage difference

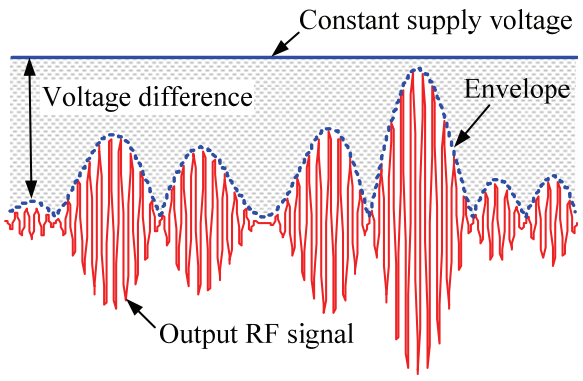

Fig. 2. Key waveforms of the LPA in 3G and 4G mobile communication systems.

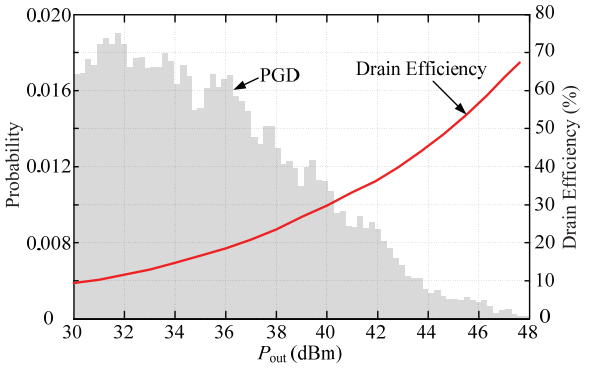

Fig. 3. DE curve of the LPA when powered by 28 V constant voltage and PGD of the RF output signal versus the output power.

between the supply voltage and output RF signal is very large.

Fig. 3 shows the curve of the drain efficiency (DE) versus the output power P_{out} of a real class AB LPA when powered by a 28 V constant voltage [4]. As seen, when the LPA outputs 47 dBm power, the DE reaches 65%. However, the DE drops quickly with the output power backing off. For example, the DE falls to 10% when the LPA outputs 30 dBm power. Fig. 3 also gives the power generation distribution (PGD) of the output RF signal with 8.5 dB PAPR when the LPA outputs a 40 dBm average power. Obviously, the probability that the LPA works at its low efficiency region is large. As a result, the average efficiency of the LPA is about 30%, and a large portion of energy is wasted.

In order to improve the efficiency of the LPA at the power back-off region, many techniques have been proposed. Among these techniques, Doherty technique [5]-[12], envelope elimination and restoration (EER) technique [13]-[20] and envelope tracking (ET) technique [21]-[28] are the most popular, and the ET technique is found to be the most promising for future mobile communication systems. The basic idea of the ET technique is to modulate the supply voltage of the LPA to track the envelope of the RF signal, and thus, the DE of the LPA is improved. Such power supply in the ET technique is usually called ET power supply. With the development of the mobile communication systems, the bandwidth and PAPR of the envelope signal is increasing, imposing stringent challenges for the design of the ET power supply.

As well known, switched-mode converter is featured with high efficiency compared with linear amplifier, and it is preferred to construct the ET power supply. However, when the bandwidth of the envelope signal is too high, the switched-mode converter should be operated at a very high switching frequency, resulting large switching loss and thus degrading the efficiency. As a result, the switching loss or the switching frequency needed to track the broadband envelope signal should be minimized for achieving a high efficiency.

The objectives of this paper are to reveal the essential reason why the LPA is less efficient in modern mobile communication systems, the superiorities of the ET technique, and how to build an ET power supply with high efficiency and wide bandwidth from the aspect of structure and control strategy. Our previous works [29], [30] have addressed these issues, and more detailed analyses are added in this paper. This paper is organized as follows. Section II presents the operating principle of the Doherty, EER and ET techniques, the pros and cons of each technique are analyzed, and it is pointed out that ET technique is the most promising technique of enhancing the efficiency of the LPA in future mobile communication systems. In Section III, the existing ET power supplies are classified into three types and detailed comparison is presented. In Section IV, the methods aiming for increasing the efficiency of the ET power supply are given, and the operating mechanisms are illustrated. Finally, Section V concludes this paper.

II. Efficiency Enhancement Techniques for Power Amplifier

As illustrated above, the LPA supplied by constant voltage suffers from low efficiency when amplifying RF signals with large PAPR. Thus, advanced PA techniques have been proposed to achieve high efficiency and satisfy the linearity requirement simultaneously. In this section, the popular advanced PA techniques, including the Doherty technique, EER technique, and ET technique, will be discussed.

A. Doherty Technique

The Doherty technique was invented by William H. Doherty in 1936 [5]. Fig. 4 shows the schematic diagram of the even Doherty amplifier, which is composed of a splitter, a carrier amplifier, a peak amplifier, and three quarter-wave transmission lines (line 1, line 2, and line 3). The carrier amplifier is realized by a LPA to satisfy the linearity requirement of the output RF signal. In order to enhance the efficiency of the carrier amplifier at power back-off region, the peak amplifier, which is realized by a NLPA due to its high efficiency, and line 1 are employed to modulate the load resistance of the carrier amplifier by active load-pull technique. Since line 1 introduce 90° phase shift to the output RF signal from the carrier amplifier, line 2 is added to the RF path of the peak amplifier to balance the phase shift. Meanwhile, line 3 is

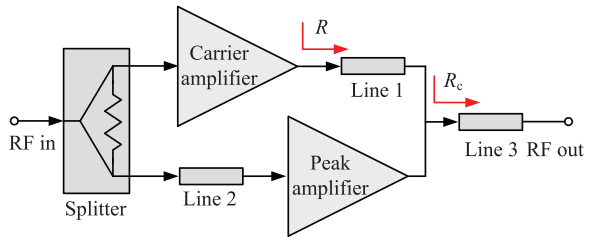

Fig. 4. Schematic diagram of the even Doherty amplifier.

added to realize impedance transformation because the output impedance of a typical RF system is 50 Ohm.

The RF input signal is split into two parts by the splitter. When the input power is low, only the carrier amplifier works, and the peak amplifier is shut down. While increasing the input power level to 6 dB power back-off from the maximum RF input power, carrier amplifier and peak amplifier work together.

Here, a class B power amplifier is taken as the carrier amplifier to explain the operating principle of the Doherty technique. Fig. 5 shows the circuit of class B power amplifier, where C_{block1} and C_{block2} are the dc blocking capacitors, L_{choke1} and L_{choke2} are the RF chokes, v_{gs} is the driving signal, V_{th} is the threshold voltage of the power amplifier, i_d is the drain current, v_{ds} is the drain voltage, V_{DC} is the dc power supply of the power amplifier, and R is the load resistance of the power amplifier, as given in Fig. 4.

Fig. 6 shows the voltage and current waveforms and load lines of class B power amplifier. Since the power amplifier is biased at class B, i_d is a half-rectified sine wave, and its fundamental component I_1 when the maximum drain current is I_{max}, as shown in Fig. 6(a), can be expressed as

$$I_1 = I_{max}/2 \tag{1}$$

And the DC component I_0 of i_d can be expressed as

$$I_0 = I_{max}/\pi \tag{2}$$

The DE can be calculated by dividing the RF fundamental output power, P_1, by the input power from V_{DC}, P_{DC}. Thus, according to (1) and (2), the DE can be calculated by

$$\mathrm{DE} = \frac{P_1}{P_{DC}} = \frac{V_1 \cdot I_1}{V_{DC} \cdot I_0} = \frac{\frac{V_{DC}}{\sqrt{2}} \cdot \frac{I_{max}}{2\sqrt{2}}}{V_{DC} \cdot \frac{I_{max}}{\pi}} = \frac{\pi}{4} \tag{3}$$

It can be seen from (3) that, the full driven class B power amplifier, as shown in Fig. 6(a), can achieve $\pi/4$ efficiency theoretically.

Fig. 6(b) shows the key waveforms of the class B power amplifier when the input RF power decreases 6 dB (one-fourth of maximum power) when compared with Fig. 6(a). At this time, the peak current of i_d and voltage swing of v_{ds} are halved, and the I_1 and I_0 can be expressed as

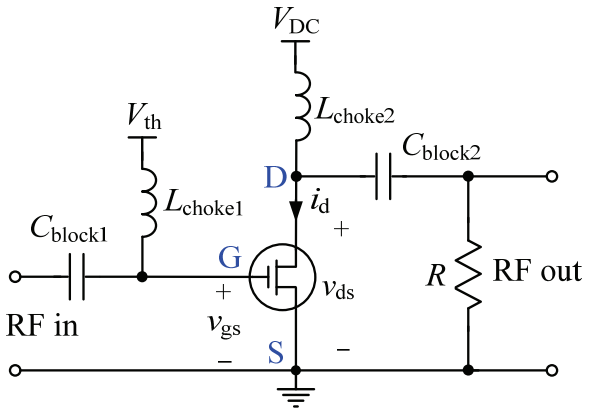

Fig. 5. Circuit of class B power amplifier.

$$I_1 = I_{max}/4 \tag{4}$$

$$I_0 = \frac{I_{max}}{2\pi} \tag{5}$$

According to (4) and (5), the DE can be expressed as

$$\mathrm{DE} = \frac{P_1}{P_{DC}} = \frac{V_1 \cdot I_1}{V_{DC} \cdot I_0} = \frac{\frac{V_{DC}}{2\sqrt{2}} \cdot \frac{I_{max}}{4\sqrt{2}}}{V_{DC} \cdot \frac{I_{max}}{2\pi}} = \frac{\pi}{8} \tag{6}$$

Comparing (3) and (6), it can be seen that the DE of the traditional class B power amplifier decreases with power backing off.

The load resistance of the class B power amplifier in Fig. 6(a) and (b) is R, while the load resistance is $2R$ in Fig. 6(c). Comparing Fig. 6(b) and (c), the peak current of i_d is the same since the input power is identical. However, the voltage swing of v_{ds} in Fig. 6(c) is increased due to the increased load resistance. At this time, the DE can be expressed as

$$\mathrm{DE} = \frac{P_1}{P_{DC}} = \frac{V_1 \cdot I_1}{V_{DC} \cdot I_0} = \frac{\frac{V_{DC}}{\sqrt{2}} \cdot \frac{I_{max}}{4\sqrt{2}}}{V_{DC} \cdot \frac{I_{max}}{2\pi}} = \frac{\pi}{4} \tag{7}$$

It can be seen from (7) that, when the input RF power is small, increasing the load resistance could increase the DE, as shown in Fig. 6(c), which is the mechanism of the Doherty technique. In conclusion, when the input RF power is small, the carrier amplifier should have high load resistance to achieve a high DE. However, the load resistance decreases with the increased input RF power. In order to adjust the load resistance according to the input RF power, the active load-pull technique is adopted.

Fig. 7 shows the simplified schematic diagram of the Doherty amplifier to illustrate the operating principle of the active load-pull technique, where CS1 and CS2 are two current sources, representing the carrier amplifier and peak amplifier, respectively, R_c is the common load of the carrier

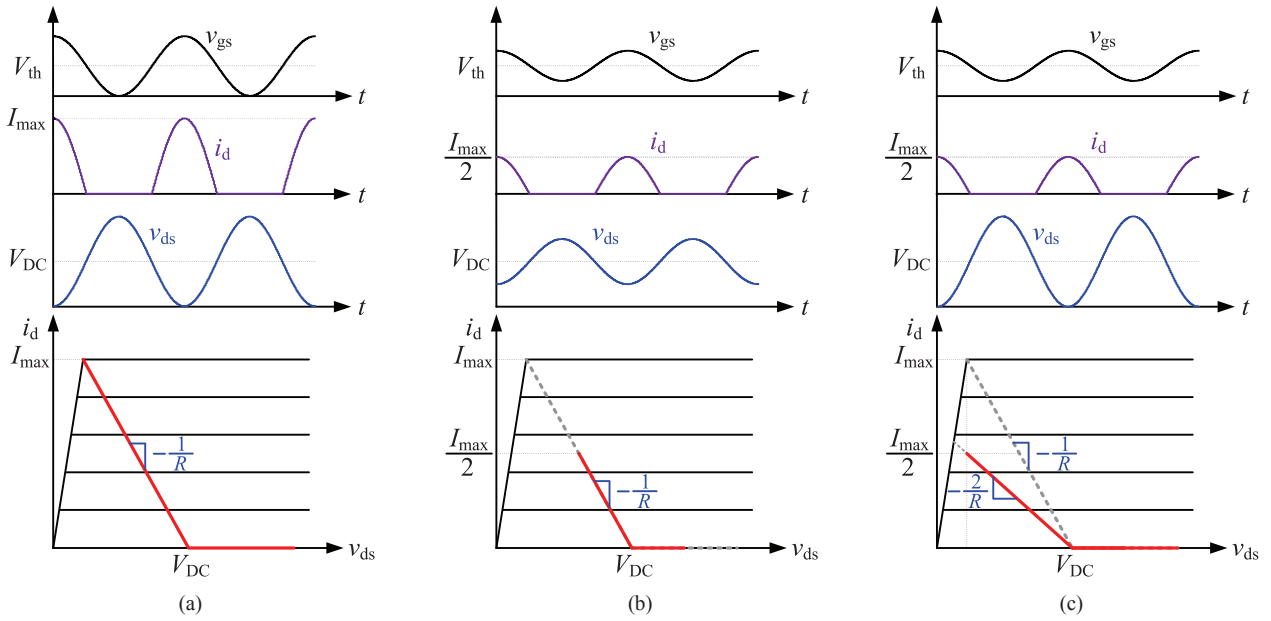

Fig. 6. Voltage and current waveforms and load lines of class B power amplifiers. (a) Full driven with load resistance R. (b) 6 dB back-off with load resistance R. (c) 6 dB back-off with load resistance $2R$.

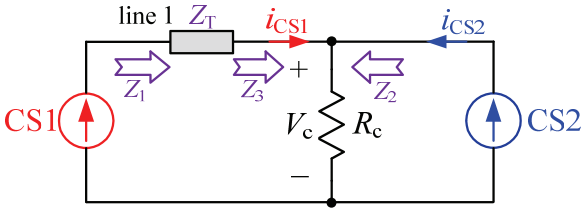

Fig. 7. Active load-pull technique.

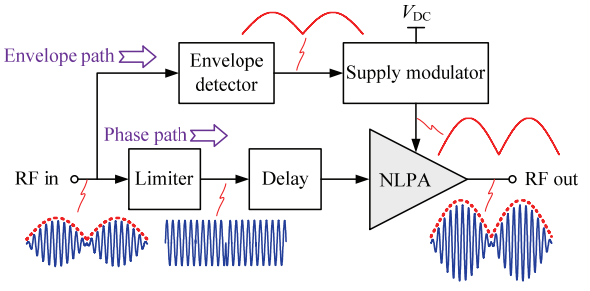

Fig. 8. Schematic diagram and key waveforms of EER technique.

amplifier and peak amplifier, as shown in Fig. 4, and Z_T is the impedance of line1.

According to Fig. 7, V_c can be expressed as

$$V_c = R_c \cdot (i_{CS1} + i_{CS2}) \tag{8}$$

Thus, the resistance Z_3 can be expressed as

$$Z_3 = \frac{R_c \cdot (i_{CS1} + i_{CS2})}{i_{CS1}} = R_c \cdot \left(1 + \frac{i_{CS2}}{i_{CS1}}\right) \tag{9}$$

Based on the characteristics of the quarter-wave transmission line [4], we have

$$Z_1 = \frac{Z_T^2}{Z_3} \tag{10}$$

Thus, the load resistance of CS1, Z_1, can be adjusted by i_{CS2}, and Z_1 decreases with the increase of i_{CS2}.

B. EER Technique

EER technique was first invented by Leonard R. Kahn in 1952 [13] and received lots of attention ever since. Fig. 8 shows the schematic diagram and key waveforms of the EER technique. The RF input signal, which includes both amplitude and phase information, is processed by two paths, namely, the envelope path and the phase path. In the envelope path, the envelope of the RF input signal is detected by the envelope detector and serves as the reference voltage of the supply modulator. The supply modulator outputs a voltage that tracks the envelope of the RF input signal and supplies the nonlinear power amplifier (NLPA). In the phase path, the envelope information of the RF input signal is eliminated by the limiter, producing a signal with constant amplitude and only containing the phase information of the RF input signal. The amplitude information is restored by the supply voltage provided by the supply modulator. The delay unit is used to synchronize the envelope path and the phase path.

Since a NLPA is adopted in EER technique, a high efficiency can be achieved. By introducing the supply modulator to modulate the supply voltage of the NLPA, the NLPA works like a high efficient LPA.

C. ET Technique

Fig. 9 shows the schematic diagram and key waveforms of the ET technique, which is similar to EER technique. The

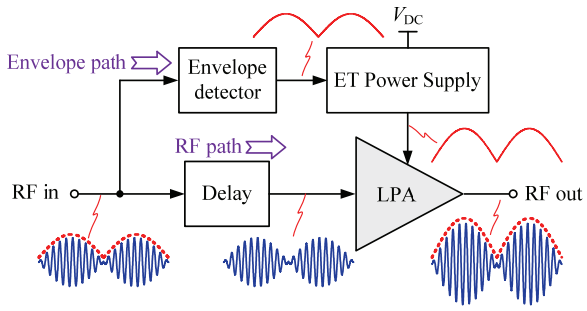

Fig. 9. Scheme diagram and key waveforms of ET technique.

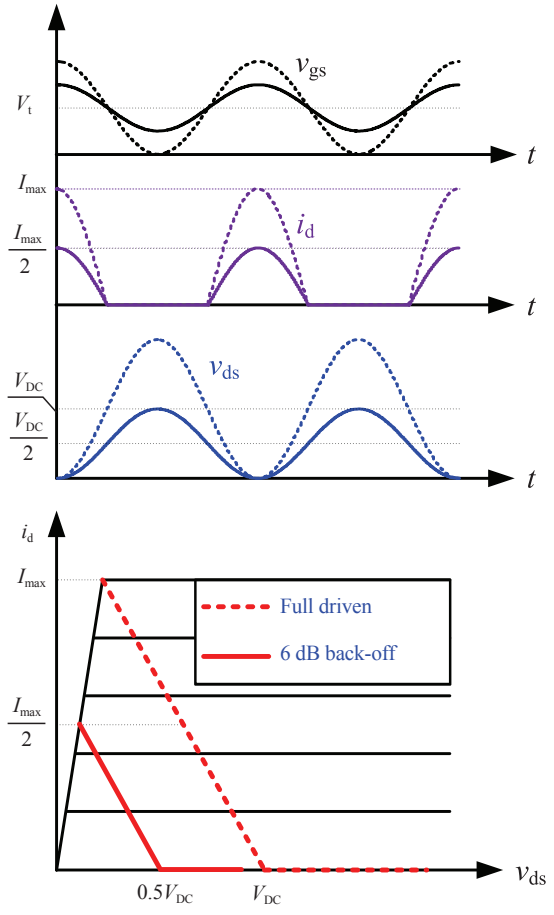

Fig. 10. Voltage and current waveforms and load lines of class B power amplifiers using ET technique at different power levels.

main differences between them can be summarized as: 1) a LPA is adopted in the ET technique, while a NLPA is used in the EER technique; 2) the RF signal amplified by the power amplifier includes both the amplitude and phase information in the ET technique, while the RF signal just contains phase information in EER technique; 3) The function of the supply modulator in EER technique is to restore the amplitude information of the output RF signal, while the ET power supply in ET technique aims for enhancing the efficiency of the LPA.

Fig. 10 shows the key waveforms of the class B power amplifier using ET technique at different power levels. When

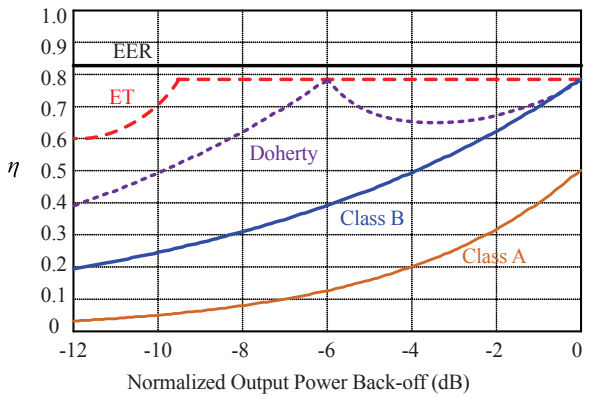

Fig. 11. Efficiency curves of power amplifiers using different techniques versus normalized output power back-off.

the class B power amplifier is full driven, as shown with the dotted lines, its efficiency can reach $\pi/4$. When the input RF power backs off, the ET power supply outputs a lower voltage to supply the LPA correspondingly. The solid lines present the key waveforms of the class B power amplifier when the input power has a 6 dB back-off. At this time, the DE can be expressed as

$$\mathrm{DE} = \frac{P_1}{P_{DC}} = \frac{V_1 \cdot I_1}{V_{DC} \cdot I_0} = \frac{\frac{V_{DC}}{2\sqrt{2}} \cdot \frac{I_{max}}{4\sqrt{2}}}{\frac{V_{DC}}{2} \cdot \frac{I_{max}}{2\pi}} = \frac{\pi}{4} \tag{11}$$

From (11), the ET technique can also achieve a high DE at the power back-off region by dynamically adjusting the supply voltage of the LPA.

D. Comparison of the Three Techniques

Fig. 11 shows the efficiency curves of the amplifiers using different techniques, where the class A and class AB power amplifiers are powered by constant voltage. As seen, the Doherty, EER, and ET techniques are all capable of enhancing the efficiency of the power amplifier at the power back-off region. The power amplifier in the EER technique can achieve the highest efficiency, which could exceed 80% due to the adoption of NLPA. The LPA in ET technique could achieve 78.5% efficiency at high output power level when the LPA is biased at class B, and the efficiency decreases at low output power region due to the adoption of the envelope shaping [31]-[33], which results in the amplitude of the shaped envelope signal is higher than that of the original envelope signal. The efficiency curve of the Doherty amplifier is piecewise. At low output power region (< −6dB), the peak amplifier shuts down, the carrier amplifier works with a large load resistance, leading to a higher efficiency than traditional class B power amplifier. At high output power region (> −6dB), the carrier and peak amplifiers works together, and the efficiency keeps high.

Many mobile communication operators adopt Doherty technique in their base stations due to the simple structure.

TABLE I
COMPARISON OF DOHERTY, EER, AND ET TECHNIQUES

	Doherty	EER	ET
Power amplifier	LPA (Carrier amplifier) NLPA (Peak amplifier)	NLPA	LPA
Applications	Narrow-band	Medium	Broadband
Efficiency	Medium	Highest	High
Linearity	Medium	Good	Good
Delay matching	/	Tighter	Tight
Requirement to supply modulator	/	High	Medium

However, the Doherty technique has several disadvantages: 1) it needs two power amplifiers, leading to increased cost; 2) at low output power region, the efficiency of the Doherty amplifier decreases quickly with output power backing off, which results in low efficiency when amplifying signals with very large PAPR; 3) it needs quarter-wave transmission lines to realize impedance transformation, which restricts its application in broadband application; and 4) since the peak amplifier is implemented with a NLPA, the linearity of the Doherty amplifier at high output power level is sacrificed. In conclusion, the Doherty amplifier is suitable for medium PAPR and narrow-band application, and can not meet the requirement of future mobile communication systems.

The EER technique could achieve the highest efficiency. However, EER technique also has some problems: 1) since the amplitude information is restored by the supply modulator, the linearity of the system completely lies on the linearity of the supply modulator, which imposes great challenges for the design of the supply modulator; 2) the linearity of the system is very sensitive to the delay matching between the envelope path and the phase path, and any mismatching between them will result in distortion of the RF output signal; 3) the EER system has a low gain in the low-power region and results in a poor linearity; and 4) the limiter will extend the bandwidth of the RF input signal, which poses challenges on the design of the broadband limiter and power amplifier. All of these issues limit its application.

Comparing with the EER technique, the linearity of the ET system is mainly determined by the LPA, thus the linearity requirement of the ET power supply are not so stringent, which makes the selection of its output voltage flexible. Thus, the requirement to the bandwidth of the ET power supply could be lowered. Meanwhile, the accuracy of the delay matching between the envelope path and RF path in ET technique could be decreased without bringing distortion to the RF output signal. These advantages make ET technique more suitable for broadband application. Besides, the ET technique has a higher gain in low output power region with envelope shaping, which avoids gain collapse and improves the linearity of the system.

TABLE I shows the detailed comparison of these three efficiency enhancement techniques, and the ET technique is the most promising technique for future mobile communication systems due to easily implementation and suitable for broadband application.

TABLE II
THE PAPR AND BANDWIDTH OF THE ENVELOPE SIGNALS FOR DIFFERENT MOBILE COMMUNICATION SYSTEMS

Communication system		PAPR (dB)	Bandwidth (MHz)
2G	GSM	0	
2.5G	EDGE	3.2	0.2
3G	CDMA2000	3.5 ~ 9	1.25
	WCDMA		5
	TD-SCDMA		1.6
4G	LTE	8.5 ~ 13	2.4 ~ 20

III. ET POWER SUPPLIES

ET power supply is the core of the ET technique and plays a crucial role in the efficiency of the ET system η_{ET}. According to Fig. 9, η_{ET} can be approximated as

$$\eta_{ET} = \eta_{PS} \cdot \eta_{LPA} \tag{12}$$

where, η_{PS} is the efficiency of the ET power supply, and η_{LPA} is the efficiency of the LPA.

In order to achieve a high η_{ET}, the ET power supply is expected to achieve a high efficiency itself. Besides, the ET power supply should have a higher bandwidth than the envelope of the RF input signal so that its output voltage can well track the envelope to guarantee the LPA can achieve high efficiency. In conclusion, the ET power supply should achieve both wide bandwidth and high efficiency. TABLE II gives the PAPR and bandwidth of the envelope signal for different mobile communication systems. As seen, with the development of mobile communication systems, the PAPR and bandwidth of the envelope signal are increasing, imposing the challenges for designing the ET power supply.

Various structures of the ET power supply have been presented in previous publications, which can be classified into three categories, namely, linear amplifier structure [34], [35],

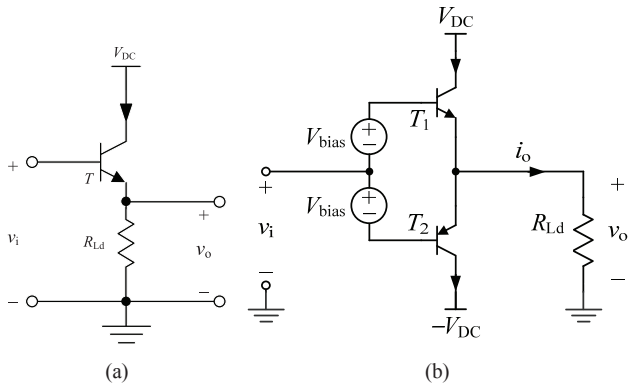

Fig. 12. Circuits of typical linear amplifiers. (a) Class A. (b) Class AB.

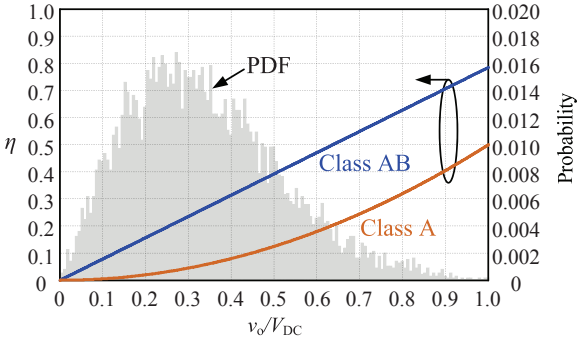

Fig. 13. Efficiency curves of the linear amplifiers and PDF of the envelope signal versus normalized output voltage.

switched-mode converter structure [36]-[42], and switch-linear hybrid (SLH) structure [43]-[50].

A. Linear Amplifier Structure

Fig. 12 shows the circuits of typical linear amplifiers, where the LPA is represented by R_{Ld} here since it can be equivalent to a constant resistor when supplied by the ET power supply [21]. Fig. 12(a) shows the circuit of class A linear amplifier, where T is the power device. The class A linear amplifier can output unidirectional voltage and current, and its theoretical maximum efficiency is 50%. Fig. 12(b) shows the circuit of the class AB linear amplifier, where T_1 and T_2 are the power devices, and V_{bias} is the bias voltage to avoid crossover distortion. T_1 conducts in the positive part of the input signal, and T_2 conducts in the negative part. The class AB linear amplifier can output unidirectional voltage and bidirectional current, and its theoretical maximum efficiency is 78.5%.

The linear amplifiers feature with high bandwidth and small output voltage ripple, and they have good ability of tracking the envelope signal, guaranteeing that the LPA achieves high efficiency and no spectrum disturbance occurs. Fig. 13 shows the efficiency curves of the linear amplifiers and probability density distribution (PDF) [28] of the envelope signal with 8.5 dB PAPR. It can be seen that the efficiencies of the linear amplifiers decrease with the output voltage. Referring to the PDF curve, there is a large probability that the envelope signal lies in the low amplitude region, where the linear amplifier is less efficient. More than that, the PDF would move left if the PAPR of the envelope signal becomes higher, and this would further worse the efficiency of the linear amplifiers. In future mobile communication systems, the PAPR will be continuously increased, and the ET power supply using the linear amplifier structure is not efficient.

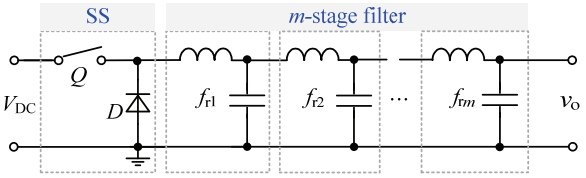

Fig. 14. Buck converter with m-stage filters.

B. Switched-Mode Converter Structure

The switched-mode converter can achieve high efficiency and it is preferred to construct the ET power supply. According to the number of power switches used, the switch network can be classified into single-switch (SS) network and multiple-switch (MS) network. Therefore, the switched-mode converter structure can be categorized as SS Structure and MS Structure. For the base station application, a step-down converter is needed, and an open-loop controlled buck converter is usually employed to be a ET power supply or a basic cell due to its simple structure [39]-[41]. The following analysis is on the basis of the buck converter, and the analysis can be extended to other converters.

1) SS Structure

Fig. 14 shows the circuit of the buck converter with m-stage filter. Each stage filter is composed of an inductor and a capacitor, and the resonant frequency of each stage filters are $f_{r1}, f_{r2}, ..., f_{rm}$, respectively.

When m = 1, the circuit shown in Fig. 14 will be a traditional buck converter. For the purpose of attenuating the switching frequency component, the resonant frequency f_{r1} should be far below the switching frequency f_s, i.e., $f_{r1} << f_s$. The attenuation at the switching frequency, $A_1(f_s)$, can be expressed as

$$A_1\left(f_s\right) = -40 \cdot \log\left(\frac{f_s}{f_{r1}}\right) \tag{13}$$

When the buck converter is open-loop controlled, its bandwidth f_{BW} approximately equals to f_{r1}, i.e., $f_{BW} \approx f_{r1}$. Therefore, $f_{BW} << f_s$. In order to track the envelope signal with wide bandwidth, the switching frequency of the SS structure should be very high. For example, if f_{BW} = 20 MHz, f_s is required to be higher than 200 MHz. For such a high switching frequency, the traditional silicon-based power switches will suffer significant switching loss, greatly degrading the efficiency of the ET power supply. Fortunately, gallium nitride (GaN) high electron mobility transistors (HEMTs) emerged, which are suitable for operating at very high frequency with

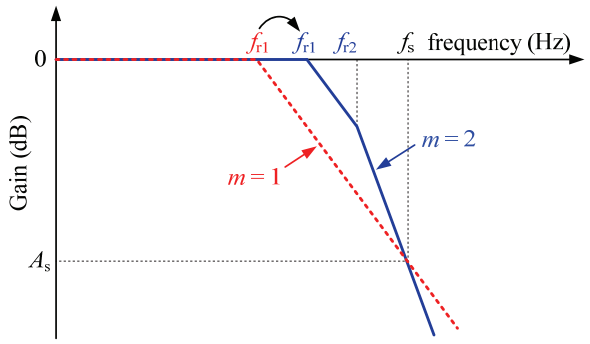

Fig. 15. Gain curves versus frequency of the single-stage and two-stage filters.

smaller switching loss [51]-[54]. When operating at such a high switching frequency, the parasitic parameters of the packaging and PCB layout have great impacts on the performance of the ET power supply. In order to effectively decrease the undesired parasitic parameters, the control circuits and the power devices are preferred to be integrated into a single chip [55], [56].

In order to track the envelope signal with reduced f_s, m-stage filter ($m > 1$) can be used. At this time, the attenuation at the switching frequency $A_m(f_s)$ can be expressed as

$$A_m(f_s) = -40 \cdot \log\left(\frac{f_s}{f_{r1}}\right) - 40 \cdot \log\left(\frac{f_s}{f_{r2}}\right) - \ldots - 40 \cdot \log\left(\frac{f_s}{f_{rm}}\right) \quad (14)$$

Fig. 15 shows the gain curves versus frequency of the single-stage and two-stage filters. It is clear to see that the minimum resonant frequency, f_{r1}, of the two-stage filters can be pushed closer to f_s for the same attenuation effect at f_s, which is higher than that of the single-stage filter. Therefore, the bandwidth of the SS structure using m-stage filter ($m > 1$) can be increased. However, as m increases, the design of the filter network is very complicated. Usually, $m = 2$ is selected.

2) MS Structure

The purpose of the MS structure is to increase the equivalent switching frequency f_{e_s}. So, the frequency component needed to be suppressed is located at nf_s, where n is the number of switches used in the switch network. If the attenuation effect at f_{e_s} is the same with the attenuation effect at f_s in SS structure, the resonant frequency of the filter in MS structure, f_{e_r1}, will be n times f_{r1}. Also, when the MS structure is open-loop controlled, its bandwidth f_{BW_MS} approximately equals to f_{e_r1}. So, we have $f_{BW\_MS} \approx f_{e\_r1} = n f_{r1}$. This means that, compared with the SS structure, the bandwidth of MS structure, f_{BW_MS}, can be increased by n times.

Fig. 16 shows the schematic diagrams of typical MS structures, including the multilevel MS [44] and multiphase MS [54]. Fig. 16(a) shows a typical implementation of the multilevel MS structure, which is composed of a level provider and a level selector. The level provider generates a series of voltage levels V_1, V_2, …, V_n ($V_1 < V_2 < \ldots < V_n = V_{DC}$). As all the voltage levels share the same ground, the level provider

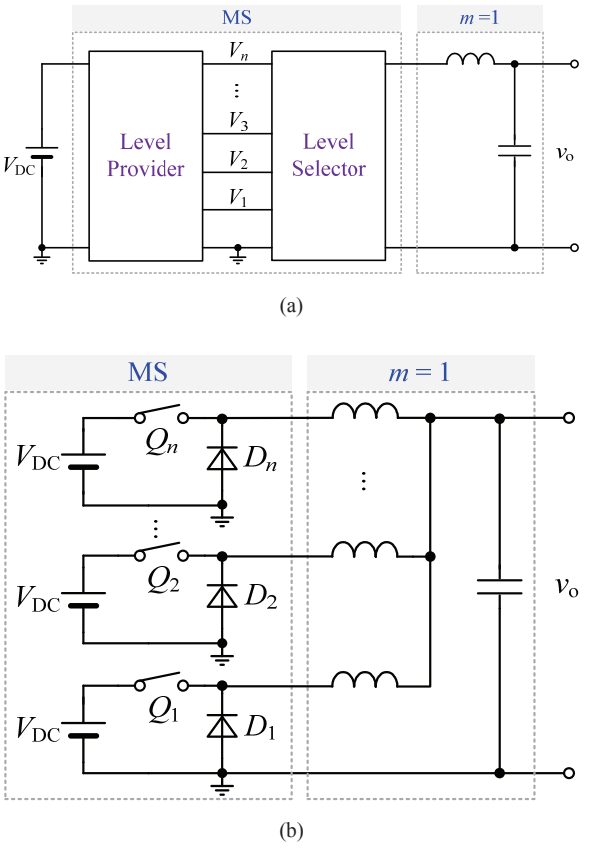

Fig. 16. Schematic diagrams of typical MS structures. (a) Multilevel MS. (b) Multiphase MS.

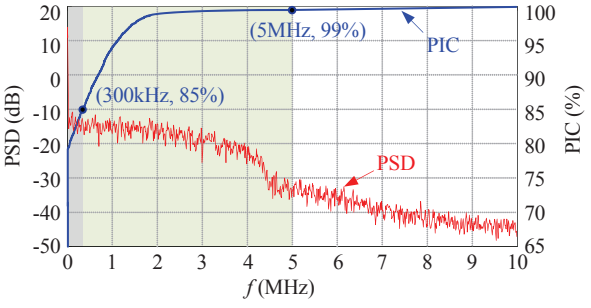

Fig. 17. PSD and PIC of the WCDMA envelope signal.

can be implemented by non-isolated dc-dc converters. The level selector chooses the corresponding voltage levels to roughly synthesize the envelope signal. Fig. 16(b) shows the schematic diagram of the multiphase MS structure. The phases are operated in an interleaved manner, thus the size of the filter network can be reduced due to the increased equivalent switching frequency and the ripple cancelation effect [49]. However, multiphase MS structure often requires a current-sharing loop to guarantee each phase providing equal power [49], which increases the system complexity and restricts the dynamic response. m-stage filter ($m > 1$) can also be applied to MS structure to further improve the bandwidth. However, the system is very complex.

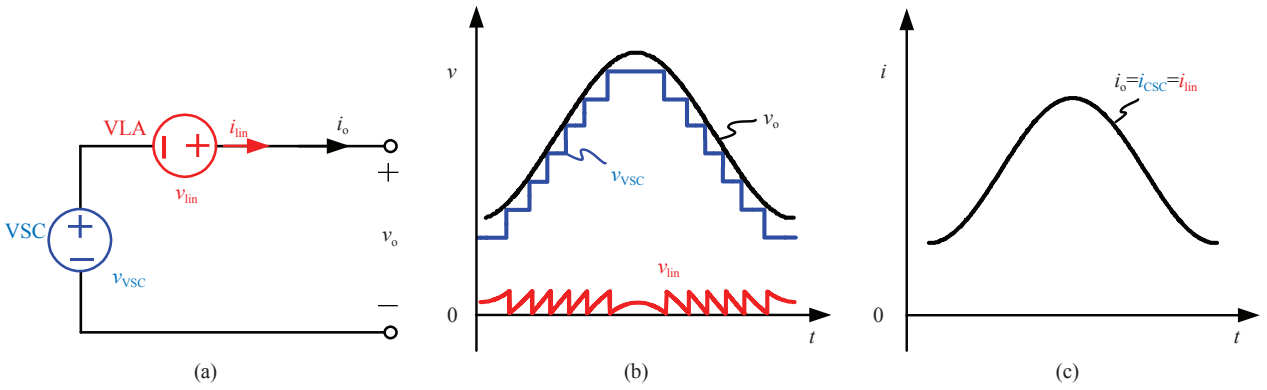

Fig. 18. Block diagram and key waveforms of series-form SLH ET power supply. (a) Block diagram. (b) Key voltage waveforms. (c) Key current waveforms.

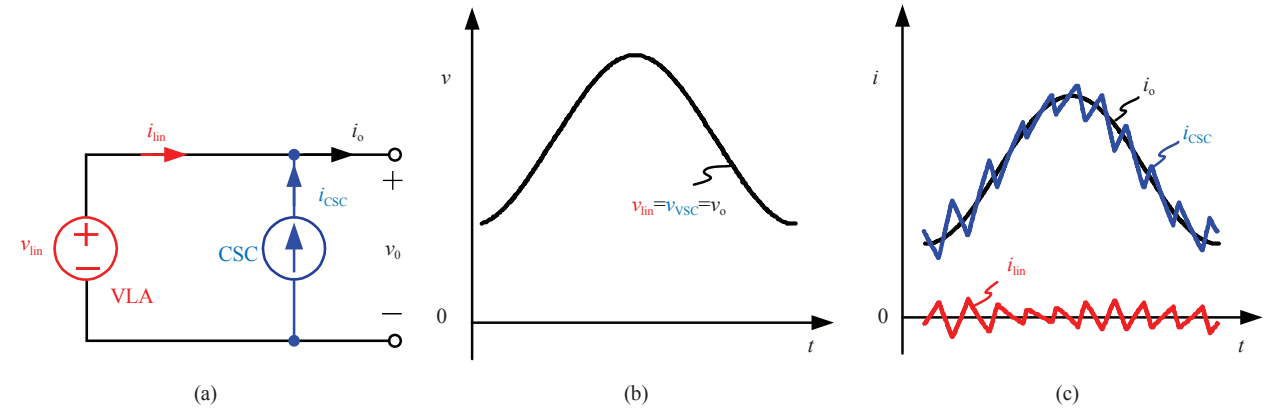

Fig. 19. Block diagram and key waveforms of parallel-form SLH ET power supply. (a) Block diagram. (b) Key voltage waveforms. (c) Key current waveforms.

C. SLH Structure

In order to track the envelope signal without distortion, the switching frequency or equivalent switching frequency of the switched-mode converter structure should be higher than the bandwidth of the envelope signal. Therefore, the required switching frequency to track a broadband envelope signal is still very high. Fig. 17 shows the power spectral density (PSD) and power integration curve (PIC) of the wideband code division multiple access (WCDMA) envelope signal. As seen, about 85% power is distributed from dc to 300 kHz and 14% power lies between 300 kHz to 5 MHz. Considering this power distribution, the SLH structure for ET power supply is proposed, in which, a switched-mode converter is used to provide the large portion low-frequency power with high efficiency, while a linear amplifier is employed to process the rest little portion high-frequency power. The SLH ET power supply integrates the advantages of the switched-mode converter and the linear amplifier, and it can achieve high efficiency and high bandwidth simultaneously. Since the switched-mode converter only processes the low-frequency components of the envelope signal, the switching frequency can be significantly reduced compared with that of switched-mode converter structure.

The SLH structure can be classified into series-form [57]-[59], parallel-form [60]-[62], and series-parallel-form [4], [48], [63].

1) Series-Form SLH

The series-form SLH ET power supply is composed of a voltage-controlled switched-mode converter (VSC) and a voltage-controlled linear amplifier (VLA), which are connected in series, as shown in Fig. 18(a). The VSC is usually implemented by a multilevel converter, as shown in Fig. 16(a), which outputs a step-wave voltage v_{VSC} to synthesize the load voltage v_o, and thus decreasing the output voltage swing of the linear amplifier, v_{lin}, as shown in Fig. 18(b). In doing so, the loss the linear amplifier is reduced, and thus the efficiency of the SLH ET power supply is greatly improved. However, the output current of the linear amplifier, i_{lin}, is still the load current i_o, as shown in Fig. 18(c), which is large and still results in relatively large loss.

2) Parallel-Form SLH

The parallel-form SLH ET power supply is comprised of a current-controlled switched-mode converter (CSC) and a VLA, which are connected in parallel, as shown in Fig. 19(a). In this form, the CSC is expected to track i_o, and the linear amplifier compensates the ripple current between i_o

TABLE III
COMPARISON OF THE ET POWER SUPPLIES WITH DIFFERENT STRUCTURES

Structure	Linear amplifier		Switched-mode converter		SLH structure		
Topology	Class A	Class AB	SS	MS	Series-form	Parallel-form	Series-parallel-form
Efficiency	Low		High		High		Higher
Linearity	Good		Medium		Good		Good
Bandwidth	Wide		Narrow	Medium	Wide		Wider
Complexity	Simple		Simple	Medium	Medium		Complex

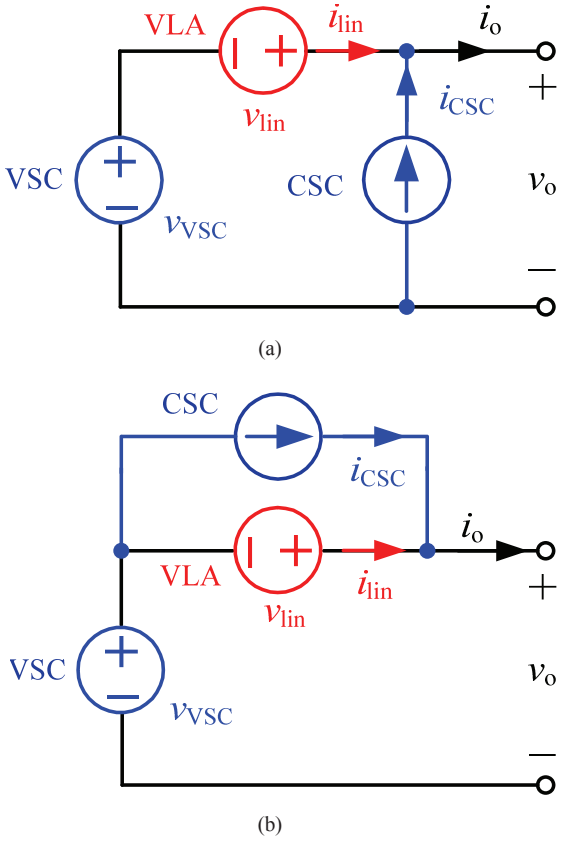

Fig. 20. Block diagram of series-parallel-form SLH ET power supply. (a) Type I. (b) Type II.

and the output current of CSC i_{CSC}, as shown in Fig. 19(c). Thus, the loss of the linear amplifier is reduced, and the ET power supply can also achieve relatively high efficiency. However, v_{lin} is equal to the load voltage v_o, as shown in Fig. 19(b), which still bring relatively large loss even if i_{lin} is small.

3) Series-Parallel-Form SLH

Regardless of the series-form or the parallel-form, the linear amplifier still has relatively large loss, which hinders the increase of the efficiency of SLH ET power supply [64]. In order to further reduce the power loss of the linear amplifier, the series-parallel-form SLH ET power supply was proposed [48], which is composed by one linear amplifier and two

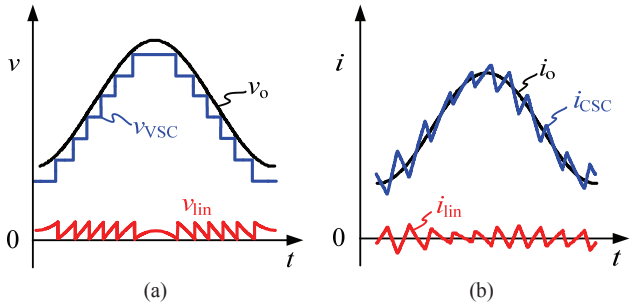

Fig. 21. Key waveforms of series-parallel-form SLH ET power supply. (a) Key voltage waveforms. (b) Key current waveforms.

switched-mode converters, which have two combinations, as shown in Fig. 20. As seen, one switched-mode converter is VSC, and the other is CSC. Fig. 21 shows the ideal voltage and current waveforms of the series-parallel-form SLH ET power supply. As seen, the i_{lin} and v_{lin} are both relatively small, leading to a reduced power loss in the linear amplifier.

TABLE III shows the comparison of the linear amplifier structure, the switched-mode converter structure, and SLH structure ET power supplies. As seen, the linear amplifier structure can achieve wide bandwidth and good linearity. However, its efficiency is relatively low. While the switched-mode converter structure features with higher efficiency and narrower bandwidth. The SLH structure combines the advantages of the linear amplifier structure and the switched-mode converter structure, and can achieve wide bandwidth and high efficiency simultaneously, and the series-parallel-form SLH structure can acquire higher efficiency and wider bandwidth due to the reduced power processed by the linear amplifier when compared with series-form and parallel-form SLH structures.

IV. METHODS OF FURTHER IMPROVING THE EFFICIENCY OF ET POWER SUPPLY

In 4G mobile communication systems, the bandwidth of the envelope signal reaches 20 MHz, and it will be as high as 100 MHz in 5G mobile communication systems. In order to track these broadband envelope signals, the switching frequency of the switched-mode converter in ET power supply should be very high, resulting large switching loss and

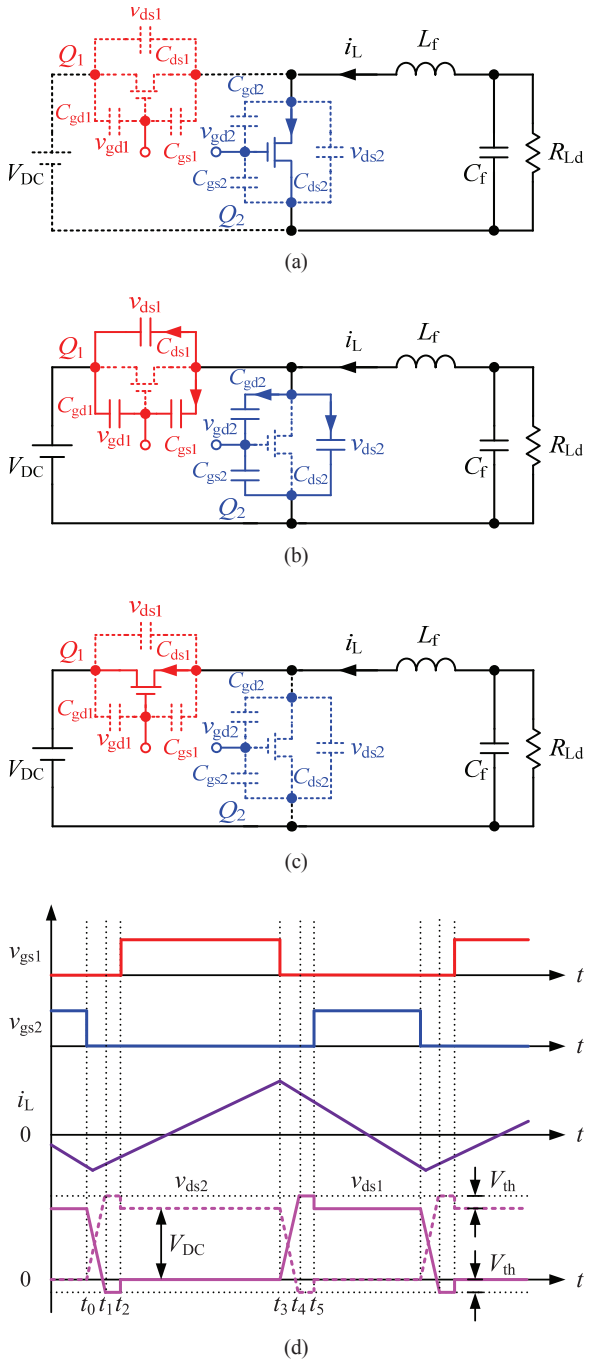

Fig. 22. Equivalent circuits and key waveforms of the buck converter. (a) Equivalent circuit before t_0. (b) Equivalent circuit during $[t_0, t_1]$. (c) Equivalent circuit during $[t_1, t_2]$. (d) Key waveforms.

thus degrading the efficiency. To achieve high efficiency, the switching loss or the switching frequency of the ET power supply should be reduced when tracking the broadband envelope signal.

A. Soft-Switching Method

To reduce the switching loss, GaN devices are preferred due to the reduced junction capacitors and fast switching frequency. Meanwhile, soft-switching method could be employed. The simple buck converter is selected to explain the operating principle of the soft-switching method. Fig. 22 shows the equivalent circuits and key waveforms of the buck converter, where Q_1 and Q_2 are the power switches, C_{ds1} and C_{ds2} are the drain-source junction capacitors, C_{gs1} and C_{gs2} are the gate-source junction capacitors, C_{gd1} and C_{gd2} are the gate-drain junction capacitors, v_{gs1} and v_{gs2} are the driving signals of Q_1 and Q_2, respectively. Noted that here the filter inductor L_f is intentionally designed to be small enough so that its current could be negative. Prior to t_0, power switch Q_2 is conducting and power switch Q_1 is turned off, the inductor current i_L decays and crosses zero, as shown in Fig. 22(a). At t_0, power switch Q_2 is turned off, and the negative inductor current i_L charges C_{gd2} and C_{ds2}, and discharges C_{gd1} and C_{ds1}, thus, v_{dg1} and v_{ds1} ($v_{dg1} = v_{ds1}$, $v_{dg1} = -v_{gd1}$) decrease and cross zero, the equivalent circuit is shown in Fig. 22(b). At t_1, v_{dg1} decays to $-V_{th}$, Q_1 conducts reversely, which provides approximate zero-voltage turn-on condition for Q_1, as shown in Fig. 22(c). The operating principle of the buck converter during $[t_2, t_5]$ is similar to that during $[0, t_2]$ and will not be explained here. As discussed above, both Q_1 and Q_2 realize zero-voltage-switching, and the switching loss is almost eliminated. The efficiency higher than 90% has been reported using GaN devices and soft-switching method [52], [53].

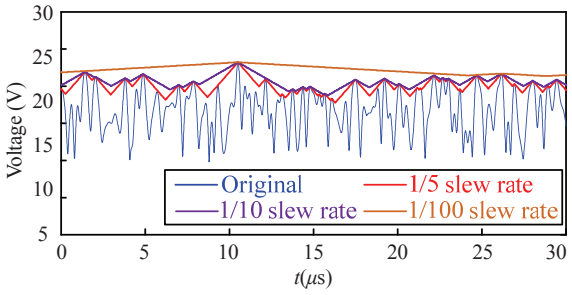

Fig. 23. Envelope signals with different slew rate.

B. Slow Envelope Method

Since the switching loss is proportional to the switching frequency, the switching loss can be decreased by reducing the switching frequency. The slow envelope method has been proposed to lower the bandwidth of the original envelope signal [65]-[67]. By replacing the original envelope signal with the slow envelope signal as the reference voltage of the ET power supply, the bandwidth of the ET power supply can be decreased, indicating a reduced switching frequency. Thus, the efficiency of the ET power supply can be improved due to the reduced switching loss.

As reported in [65], several slow envelopes are generated, as shown in Fig. 23. Fig. 24 shows the PSD of the corresponding envelope signals, and it is clear to see that the bandwidth of the envelope signal can be greatly reduced by applying slow envelope method. Thus, the requirement to the ET power supply is relieved. However, the efficiency of the LPA is sacrificed. Therefore, there is a trade-off design between the efficiencies of the ET power supply and LPA.

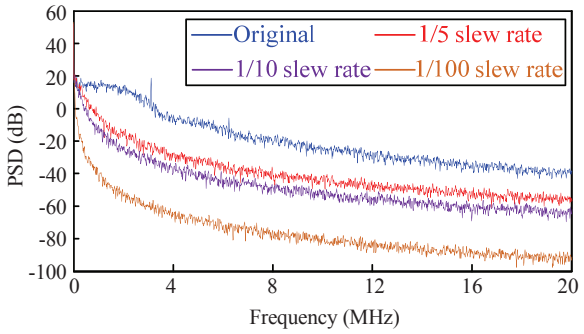

Fig. 24. Power spectral density of envelope signals with different slew rate.

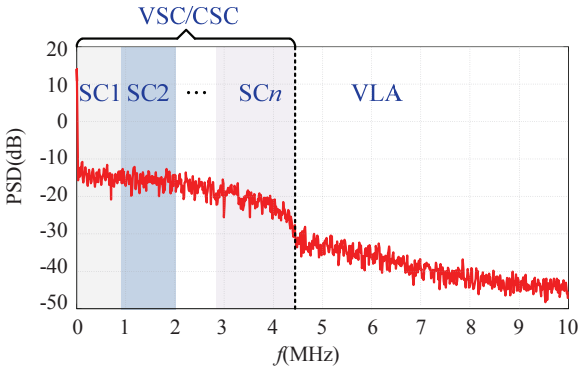

Fig. 25. Extension of band separation technique.

C. Band Separation Method

The envelope signal includes low frequency and high frequency components. In order to track the envelope signal accurately, the ET power supply should have the ability to track the high frequency components exactly, which will results in a waste of switching frequency when tracking the low frequency components. Thus, multiple converters with different tracking capability could be combined as an ET power supply to cope with different frequency components of the envelope signal, which is the basic thought of the band separation method.

The SLH structure is a representative example for applying the band separation method. The linear amplifier cooperates with the switched-mode converter to supply the frequency components of the envelope signal, i.e., the low-frequency components are processed by the switched-mode converter, while the high-frequency components are provided by the linear amplifier. The bandwidth of the switched-mode converter has a large impact on the overall efficiency. A lower bandwidth will increase the efficiency of the switched-mode converter, but the power processed by the VLA is increased with increased power loss. Therefore, the selection of the bandwidth of the switched-mode converter should trade off to achieve an overall efficiency of the ET power supply [68], [69].

Based on the SLH structure, the band separation method can be extended. Multiple switched-mode converters with different tracking capability, SC1, SC2, ..., and SC*n*, can be employed, as shown in Fig. 25, and each switched-mode converter can be optimized independently. Compared to the SLH structure with single switched-mode converter, the SLH structure with multiple switched-mode converters can achieve a higher efficiency. Since the switched-mode converters can be either voltage-controlled or current-controlled, the basic SLH structure with multiple switched-mode converters has two combinations, as shown in Fig. 26. Besides, the band separation technique can also be extended into series-parallel-form SLH structure and switched-mode converter structure.

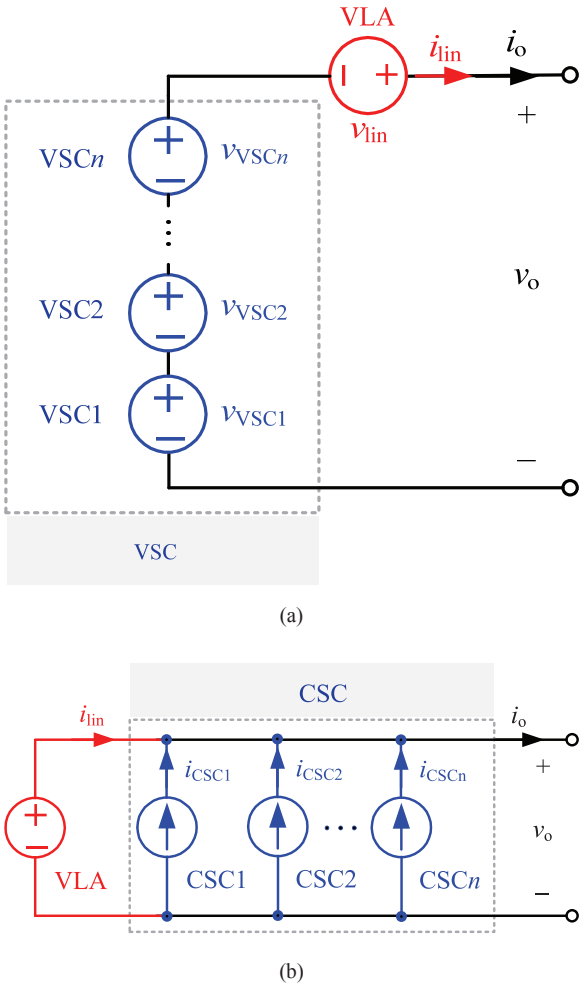

Fig. 26. SLH structures with multiple switched-mode converters. (a) Series-form SLH structure with multiple VSCs. (b) Parallel-form SLH structure with multiple CSCs.

V. Conclusion

The mobile communication systems have been continuously developing to meet the demand of high data transmission rate. Thus, spectral efficient modulation formats have been employed, which are characterized with a variable envelope of the RF signal with large PAPR. The LPAs are adopted to satisfy the strict linearity requirement of the RF output signal. However, the LPAs powered by constant volt-

age suffer from low efficiency. This paper introduces three popular efficiency enhancement techniques, i.e., Doherty, EER and ET techniques, to greatly improve the efficiency of the power amplifiers. The operating principle and characteristics of each technique are analyzed, and it is pointed out that the ET technique is the most suitable for future mobile communication systems. In the ET system, ET power supply is the core equipment and has a large impact on the system efficiency. The state-of-the-art ET power supplies are reviewed, and these ET power supplies are classified into the linear amplifier structure, the switched-mode converter structure, and the SLH structure. A comparative analysis is performed, which indicates that the SLH structure integrates the advantages of the former two structures and can achieve high efficiency and high bandwidth simultaneously. Finally, soft-switching method, slow envelope method, and band separation method, are presented aiming for further improving the efficiency of the ET power supply.

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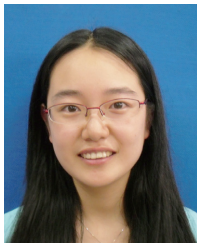

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Review of State-of-the-Art Integration Technologies in Power Electronic Systems

Kangping Wang, Zhiyuan Qi, Fei Li, Laili Wang, and Xu Yang

***Abstract*—As an important development direction of power electronic systems, the integration technologies can bring many benefits, such as size reduction, reliability improvement, cost saving and so on. With the continuous development of power semiconductor devices, especially the emergence of wide band-gap devices, more advanced integration technologies are needed. This paper reviews the state-of-art integration technologies, including active and passive integration technologies. Active integration technology is reviewed in terms of the interconnect, packaging material, packaging structure, and module integration. Passive integration technology is reviewed from the aspects of magnetic integration technology, electromagnetic integration technology, and low-temperature cofired ceramic (LTCC) technology. Higher-level integration technologies, namely power supply on chip (PwrSoC) and power supply in package (PwrSiP), are also investigated, which are mainly used in low power applications.**

***Index Terms*—Active integration, power electronic integration technology, passive integration, power module, wide band-gap device.**

I. Introduction

POWER electronics integration is a technology that integrates multiple power electronic components into a single module, which can offer many benefits such as size reduction, costs saving, and reliability improvement. In recent years, the power electronics integration technology has attracted more and more attentions, especially with the emergence of wide bandgap devices. According to device characteristics and manufacturing process, the power electronics integration technologies can be mainly classified into active integration technology and passive integration technology.

The integration of active components into a module, i.e. active integration technology, can realize low parasitics, good thermal performance, high reliability, etc. In most of available commercial power modules, the interconnections are realized by wire-bonding technology [1]-[5], shown in Fig. 1. However, this traditional packaging structure is not suitable for wide band-gap (WBG) devices which can operate at much higher frequency and temperature than Si devices [6]-[8].

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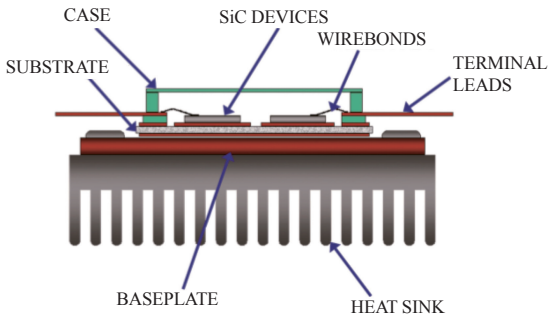


Fig. 1. Conventional wire-bonding power module structure [37].

This is because wire-bonding structure has large parasitic inductance (usually more than 10 nH) and limited heat dissipation capability [5], [9]. Besides, the lead-solder in die attachment has some drawbacks, such as low thermal conductivity, low melting point, and contamination to environment [10]-[12]. So advanced active packaging technologies involving wirebond-less interconnection technology [5], [13]-[21], advanced packaging materials [10], [22]-[26], advanced packaging structures [27]-[34] and module integration technologies [35], [36] are required to be developed.

The passive components, namely inductors, capacitors and transformers, generally occupy a large space of the total volume, which is harmful to the miniaturization of power converters. The passive integration technology, which is to integrate multiple passive components into a single module, has considerably advantages, such as size reduction and cost saving. The magnetic integration is to integrate the inductors and transformers into a single core, which has been successfully applied in some topologies, such as Cuk converter [38], forward converter [39], current-doubler rectifier [40], multiphase converter [41] and LLC converter [42], [43]. The integration of the capacitors and the magnetic components, namely the electromagnetic integration, can further reduce the number and size of the passive components. It has been implemented into LLC converters and asymmetrical half bridge circuit with current-doubler rectifier [44]. Moreover, the integration of all the components of a converter, including passive components, switches, drivers, and controllers, as a module or chip, can achieve greater improvement. Two typical examples are power supply on chip (PwrSoC) and power supply in package (PwrSiP). In recent years, the low-temperature cofired ceramic (LTCC) magnetics have gained much attentions in the 3D integration modules due to its low profile and flexible structure.

In order to break through the bottleneck of integration technologies for further improving the performance of power

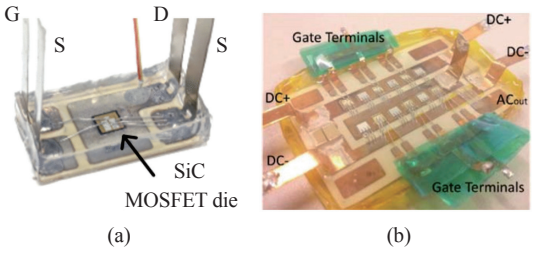


Fig. 2. Improved wire bonding based on (a) Lead frame structure [46], (b) Double-ended-sourced structure [47].

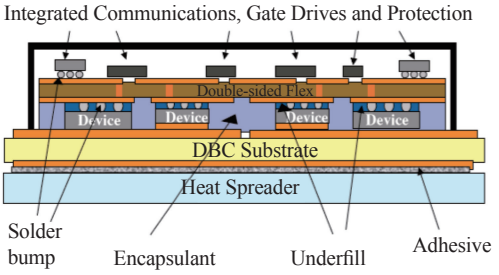


Fig. 3. Flip-Chip based module structure [20].

converters [45], this paper provides a review of the integration technologies from the aspects of active packaging integration and passive integration. Section II reviews the active integration technologies, including interconnection technology, packaging material technology, packaging structure technology, and module integration technology. Section III reviews the passive integration technologies, including the magnetic integration technology, electromagnetic integration technology, PwrSoC and PwrSiP technology, and LTCC integration technology. Section IV concludes the paper.

II. Active Integration Technologies

The integration of active devices can reduce the interconnection parasitic inductance, improve the thermal dissipation capability, reduce the cost, etc. The emergence of wide bandgap devices, such as SiC and GaN, puts higher demands on the active integration. This section will review the active integration technologies from the aspects of interconnection technology, packaging materials, advanced packaging structures, and module-level integration.

A. Interconnection Technology

The interconnection technology is to realize the connection of die to die, and die to external terminals or circuits, which is an indispensable part of packaging technology. The traditional interconnection is based on wire-bonding technology, which has large parasitic inductance, limited heat-dissipation capability and low reliability, etc. Advanced interconnection technologies, including improved wire-bonding interconnections and wirebond-less interconnections, have been developed.

1) Improved Wire-Bonding Interconnection

To utilize the advantages (such as easy realization and low cost) of conventional wire-bonding technology, advanced wire-bonding technology has been developed. In Fig. 2(a), by employing a 3D lead-frame structure, the symmetrical Kelvin Source connection for each switching device was enhanced, which can realize reduced parasitic inductance [46]. In [47], a "double-ended-sourced" busbar structure in the multi-chip module was used to realize symmetrical power loop, thus the circulating current was reduced and dynamic current was balanced, shown in Fig. 2(b). However, the power loop in these improved wirebond-less structures are still a lateral structure. In [48]-[50], a hybrid packaging structure with multilayer substrates are utilized to realize the vertical power loop with small parastics.

2) Wirebond-Less Interconnection

So far, several wirebond-less technologies have been put forward, including flip-chip technology, dimple array interconnection technology, embedded packaging technology, metal-post interconnection technology, etc.

a) Flip-Chip Technology

At the beginning, the flip-chip technology was widely used in the field of microelectronics integration, due to its low-cost, high density, and reliable interconnections [5]. This technology eliminates the wire-bonds by utilizing solder joints for interconnecting devices. Compared to conventional wire bonding package structure, flip-chip structure has reduced parasitics and improved reliability. Owing to these benefits, it is extended to power electronics applications. A flip-chip on flex (FCOF) integrated power electronics module (see Fig. 3) was proposed by John G. Bai, *et al*. in 2003 [19]. In the module, the power chips are flip-soldered on a double-sided flexible copper-clad laminate. For better thermal performance, the power chips are also soldered onto a patterned direct bond copper (DBC) substrate. Between the flex substrate and DBC substrate, an organic underfill material is filled to achieve encapsulation, which can help to reduce thermal stress and improve heat dissipation. However, this technology cannot carry large current and is not suitable for vertical power devices. This technology is expected to be used in lateral GaN modules.

b) Dimple Array Interconnection Technology

With the purpose of enhancing thermal reliability of the solder bump, Simon S. Wen developed the dimple array interconnect (DAI) technique in 2001 [14], [18], [20]. As shown in Fig. 4, the copper flex with pre-formed dimples are used to replace wire bonds as electrical interconnections. The dimpled metal interconnects enable easy forming of solder joints with the underlying devices. Smooth fillets in solder bumps can be formed to significantly reduce the thermal stresses and strains.

The solder joint always forms an hourglass-shape in the DAI processing, which suffers a very small inelastic strain during thermal cycling. Furthermore, DAI provides better thermal management, due to its simpler thermal interfaces, shorter heat dissipation path through the interconnects [14]. However, it requires a special equipment to produce and install the

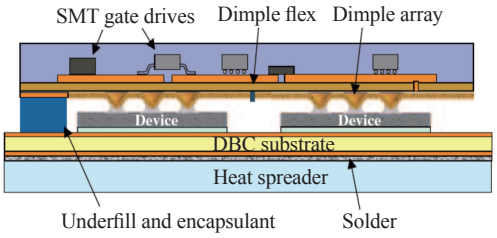


Fig. 4. DAI based module structure [20].

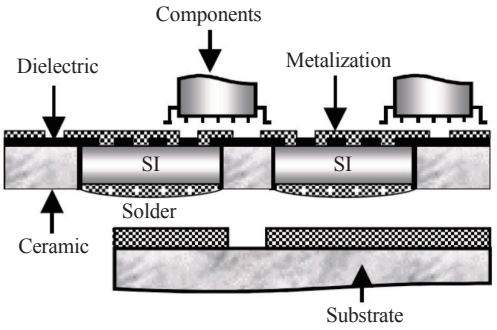


Fig. 5. Embedded power module structure [20].

copper sheet with dimple array.

c) Embedded Packaging Technology

Fig. 5 shows the conceptual embedded power packaging structure. In the structure, the embedded power devices are mounted in the openings etched out of the ceramic frame, and surrounded by an adhesive polymer. After a dielectric layer is coated on the upper surface of ceramic and power chips, via hole through the dielectric is formed on the die pad. And then the interconnections are realized by metallization on surface of the insulation layer [5], [13], [15]-[17]. The base substrate provides electrical interconnection and thermal dissipation path of power chips. This structure can realize reduced parasitics, improved power density, and low mechanical stress.

d) Metal-Post Interconnection Technology

The metal posts interconnected parallel plate structure (MPIPPS) was proposed to achieve interconnections by metal posts in [16], [18]. As shown in Fig. 6, the power chips are sandwiched between two substrates. The bottom of device is attached to the bottom plate by conventional solder die-attach processes, whereas the topside's connection to the top plane is realized through an array of metal posts. Through elimination of the wire-bonds, this technology can reduce the parasitic inductance of the interconnections.

Furthermore, MPIPPS can improve the heat dissipation capability of package due to the two directional heat transfer paths through the substrate and metal post. In addition, active heat dissipation can be implemented by filling the solid or liquid insulating thermal conductive materials in the space between parallel plates and the metal posts. In [21], the experimental results show that the maximum junction temperature of the IGBT chips in the MIPPS module is 17 °C lower than that in wire-bonding module.

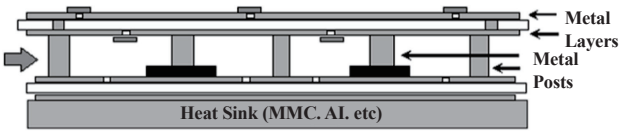


Fig. 6. MPIPPS module structure [21].

B. Packaging Material Technology

The state-of-the-art commercial power devices only can operate up to 175 ºC, which is mainly limited by packaging materials besides packaging structure. To enable WBG devices operating at high temperatures (200–350 ºC), advanced packaging materials are required to provide compatible CTE with WBG chips, and reliable high temperature performance [37]. It is essential to conduct a review of the packaging materials, which mainly include substrate materials, die-attaching materials, and encapsulation materials.

1) Substrate Materials

The substrate provides cooling, interconnection, and mechanical support for the power modules. The commonly used substrates are DBC ceramic substrate and insulating metal substrate (IMS).

In DBC ceramic substrates, Al_2O_3, AlN, BeO and Si_3N_4 can be used as the insulating materials [51]. Though BeO has the highest thermal conductive performance, it is not commonly used because the particle generated during the processing is harmful to human health. The Si_3N_4 material is also not commonly used for its low thermal conductivity and high material cost. Because the strong adhesion of substrate and copper can be easily achieved, Al_2O_3 is the most commonly used insulating materials. Compared with Al_2O_3, AlN has much higher thermal conductivity and closer CTE to SiC, but the AlN DBC substrate is costlier due to more complicated manufacturing process. With the development of manufacturing technique, AlN has the potential to replace Al_2O_3.

Generally, IMS consists of a highly thermal-conductive insulating resin sheet, a copper baseplate and thick copper foils, which can achieve good heat dissipation, and is cheaper than DBC due to the relatively simpler fabrications. IMS has been successfully applied to Mitsubishi IGBT module [37]. The life time of the module in thermal cycling has been enhanced by optimizing IMB insulating material and thickness, and a 23% increment of the effective chip-contacting area has been achieved.

2) Advanced Die-Attaching Materials

Soft solder is the most commonly used packaging material in power electronics. But its low thermal conductivity and melting point limits the power devices to operate up to 175 °C, which cannot fully exploit high temperature advantage of the WBG devices. Moreover, the lead solder is harmful to human's health and the environment, so the lead-free die-attaching materials are preferred. The nano silver sintering and transient liquid phase bonding (TLPB) are two promising alternatives.

a) Nano Silver Sintering

Nano silver sintering is a low temperature joining technique (LTJT). Due to the size effect, the melting point of silver particles in nano and micro scale is far below that of silver bulk [10], [23]-[26]. By applying a certain pressure and temperature of above 220 °C, silver particles will be melted and sintered spontaneously under the effect of liquid phase capillary force. The sintered silver has high thermal conductivity (250 W/mK), high electrical conductivity (41 MS/m) and high melting point (close to 961 °C). It has demonstrated good mechanical characteristics with a CTE value of 19 μm/mK and a tensile strength of 55 MPa. So far, silver sintering has been applied to industrial manufacturing for a range of selected products. But it is not a versatile approach for mass manufacturing mainly due to the quality issues and failures in silver-sintered contact interfaces. This sintering technique needs to be further improved.

b) Transient Liquid Phase Bonding

TLPB uses the diffusion between a high melting point and a low melting point material [19]. Many materials such as Ag/In, Ag/Sn, Au/In, Au/Sn, Cu/Sn, and Ni/Sn can be used as the soft solder with lower melting point. In the process of TLPB, the first step is to melt the low melting point material to form intermetallic phase (IMP) between the liquid and solid phase. Then after all the liquid phase transformed to IMP, a recommended maximum pressure of 0.3 MPa is required to contact the substrates while avoiding squeezing out of the liquid phase. The solid bond shows a higher remelting temperature than the initial process temperature. It has been reported that the IMC ε-phase Ag_3Sn has a melting temperature of 480 °C and the ζ-phase Ag_5Sn with a melting temperature of up to 724 °C, which are much higher than that of pure Sn with 232 °C.

3) Encapsulation Materials

Encapsulation provides protection for power module against mechanical stress, electrical breakdown, chemical erosions, α radiations, and so on. However, conventional encapsulations are only suitable for applications below 175 °C. To achieve higher operating temperature, the new encapsulation materials should have the characteristics, e.g. high thermal conductivity, close CTE to semiconductor materials, high dielectric strength, etc. Several encapsulants are reported to be able to operate above 250 °C. However, some of their properties may degrade when the temperature is close to 250 °C [52], [53]. As for underfills and molding compounds, their low glass-transition temperature (T_g) limits the high temperature operation, so appropriate modification of the chemical composition is required to achieve higher T_g. High-T_g polymers, such as polyimide, bismaleimide, and cyanate ester, are potential encapsulants for high-temperature (>250 °C) operation. However, the internal stress caused by mismatching CTE with semiconductors needs to be limited. Potting compounds limited by their thermal decomposition also need appropriate modification to improve thermal stability [11].

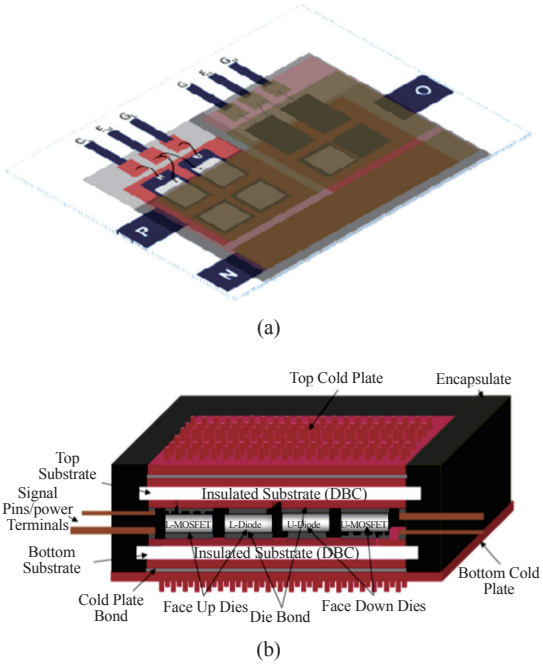


Fig. 7. Integrated double-sided cooling packaging structure [29]. (a) Aerial view of a planar-bond-all phase leg power module. (b) Cross sectional view of the module with dual cold plates.

C. Advanced Packaging Structures

In traditional power modules, a 2D layout structure is employed, in which the heat is transferred in one direction and the parasitic inductance of the interconnections are large. The more advanced structures, including 2.5D structures and 3D structures which can achieve double-sided cooling and smaller parasitic inductance, are preferred for high power density applications.

In the 2.5D structures, there are usually two substrates, one of which is for the attachment of power chips and heat sink, and the other is for interconnection [30]. In addition, copper pin, metal post or shim material is required to match the height difference between MOSFET/IGBT and diode dies [37]. The most representative packaging technology is the planar-bond-all technology which features three-dimensional planar electrical interconnection and double-sided cooling [29], [31], [32], shown in Fig. 7. The advanced packaging structure can achieve 75% reduction in parasitic inductance and 40% reduction in thermal resistance. Another typical 2.5D packaging structure is Semikron's all-sintered SKiN® package [27], [28], shown in Fig. 8. All solder and bond wire contacts are eliminated by using silver diffusion sintering joints, and the flex foil is firstly introduced for interconnections. In this structure, the parasitic inductance can be reduced up to 10%.

The 3D packaging structure is a novel concept based on stacking power dies [30], which can achieve ultra-low parasitics, compact package and excellent thermal performance. The chip-on-chip (CoC) structure proposed by Nottingham is a representative 3D structure [33], in which two power chips are vertically stacked and connected through vias,

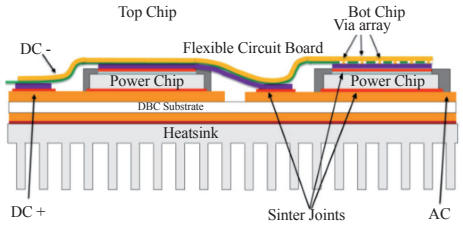


Fig. 8. SKiN® packaging structure [27].

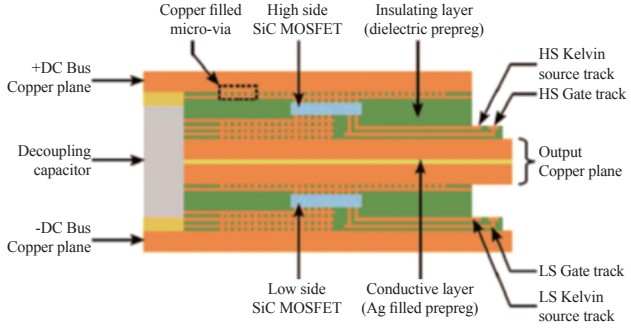


Fig. 9. CoC 3D power module structure [34].

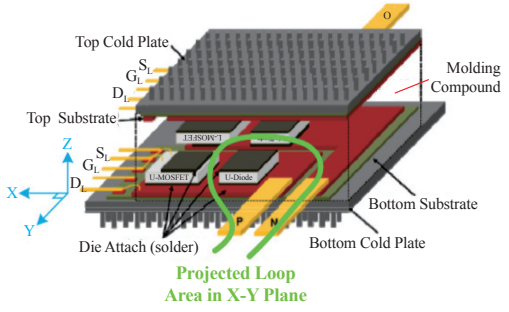


Fig. 10. Baseline power module.

copper or solder bumps etc. The 3D structure shown in Fig. 9 was proposed in [34], which demonstrates an ultra-low inductance of only 0.25 nH.

D. Module-Level Integration

Integrating the power chips with some associate components into a module can bring many benefits, such as reduced parasitics, improved thermal conductivity. The associate components which can be integrated into the module include the decoupling capacitors, gate drivers, temperature sensors, current sensors, protection circuits, etc.

The integration of decoupling capacitor is to reduce the power loop inductance by eliminating the parasitic inductance between the connection of module to external circuit. The module integrated with the decoupling capacitor shown in Fig. 11, achieves over 60% reduction of power loop parasitic inductance (just 1.63 nH) compared with the baseline module [36] in Fig. 10. The method of integrating decoupling capacitor to reduce power loop inductance was also demonstrated in [54]. Furthermore, the integration of double sided fin-pin heatsinks in Fig. 10 and Fig. 11 shows improved heat-dissipation capability.

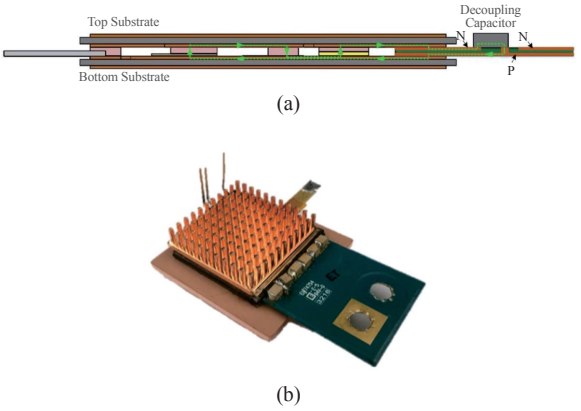


Fig. 11. Double sided cooling power module with integrated decoupling capacitor. (a) Current commutation loop illustration. (b) Fabricated power module [36].

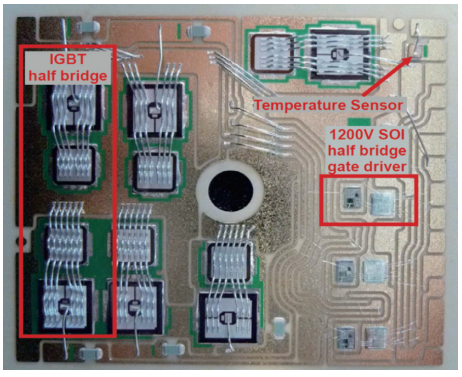


Fig. 12. A 1200 V/50 A module with integrated gate drive and temperature sensor [55].

The integration of gate driver can realize low gate loop inductance, which can reduce the gate overvoltage and ringing. [55] demonstrates a 1200 V/50 A IPM with integrated gate driver and a temperature sensor, as shown in Fig. 12. In [56], the gate driver was also integrated into a SiC half-bridge module based on the silicon-on-insulator technology. Because of the ultra-low gate loop inductance by integrating gate driver, the gate resistor can be eliminated. The integration of temperature sensor in Fig. 12 can provide the temperature information for monitoring and studying the module aging. Except the temperature sensor, current sensor can also be integrated into module. A monolithic current sensor is integrated in a SiC MOSFET module [57].

III. Passive Integration Technologies

Passive devices, especially magnetic components, often occupy a considerable volume, and become one of the main bottlenecks to improve the power density of the converters. Integrating multiple passive components can reduce their number, size and cost. This section will review some passive integration technologies, including magnetic integration technology, electromagnetic integration technology, Pwr-

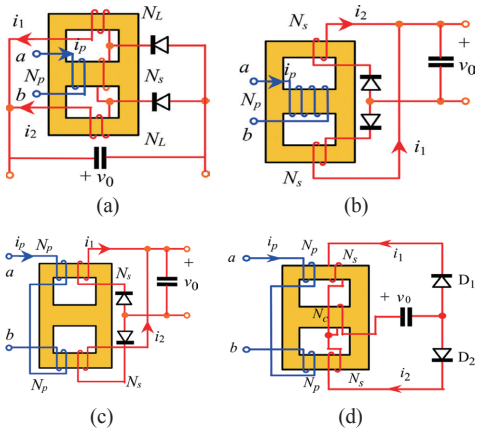


Fig. 13. Magnetic structure of CDR [61].

SOC and PwrSiP technology, and LTCC integration technology.

A. Magnetic Integration Technology

The magnetic components, namely inductors and transformers, occupy a considerable space of the total volume, which have harmful effects to the power density. To solve this problem, the magnetics are integrated into one core. There are many converters have applied the magnetic integration technology. For example, Cuk converter and forward converter are integrated into a single core by Slobodan. Cuk [38] and G. D. Bloom [39], [58], [59], respectively. An improvement of forward converter is made in [60]. The three magnetic components of the current-doubler rectifier (CDR) are integrated into single integrated component [61], shown in Fig. 13(a). To minimize the termination loss, the windings are integrated [62], shown in Fig. 13(b). An improvement is made by [63] [64]. The windings at the center leg are spilt into the two outer legs, resulting in increasing in coupling coefficient of primary and secondary, shown in Fig. 13(c). The filtering inductance in aforementioned topology has a limited value. A new design with increasing filter inductance is proposed in [65], shown in Fig. 13(d). But the increasing of the secondary windings that conduct large current, induces large winding losses. Thus, a trade-off between filter inductance and winding losses should be made. Some topologies have already implemented the integrated CDR to increase power density and reduce power losses [66], [67].

Another typical application of magnetic integration is for multiphase converter of which the inductors are integrated into one magnetics. The integrated inductors [68] can be divided into noncoupled inductors [69] and coupled inductors [70]. The integrated inverse coupled inductors can not only reduce current ripple by increasing steady state inductance, but also increase transient respond by decreasing transient inductance [41], [71]. As the interleaved phases increase, the asymmetry of the circuit as well as the complexity in design and control increase with limited benefits [72]. Although inverse coupled inductors have better performance in steady state and transient state than noncoupled inductors, winding path of coupled inductors is much larger. A twisted core coupled inductor is proposed [73], shown in Fig. 14. In [74], a lateral coupled inductor using ferrite material is proposed, shown in Fig. 15.

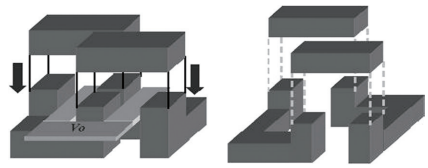


Fig. 14. Structure of the twisted core coupled inductor [73].

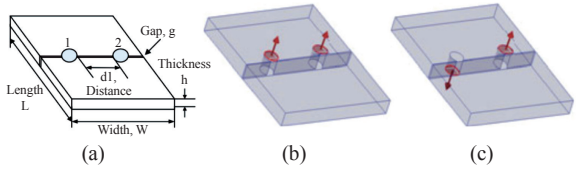


Fig. 15. Two-phase lateral-coupled inductor structure [74]. (a) Dimensions. (b) Direct coupling. (c) Inverse coupling.

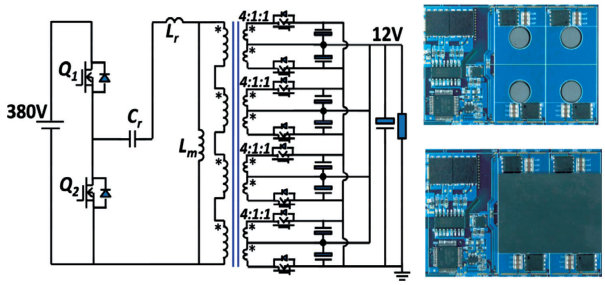


Fig. 16. Structure of integrated matrix transformer [77].

In addition, the magnetic integration is also employed in some resonant converters, such as LLC converter [42], [43]. The resonant inductor of LLC converter is realized by large leakage inductance of transformer. In order to achieving large inductance, an auxiliary core around primary windings and a low permeability layer between the primary and secondary are proposed in [43] and [42], respectively. For high output current situation, LLC converter with matrix transformer is proposed [75], [76]. The transformer consists of two cores, each of which integrates two matrix components. To further improve power density, a novel structure integrated four matrix transformer of LLC converter is proposed by CPES [77], achieving power density of 900 W/in^3, shown in Fig. 16. Shielding technique is used to reduce EMI effect of LLC converter with matrix transformer at high frequency [78].

B. Electromagnetic Integration Technology

To further reduce the number and size of the passive components, the electromagnetic integration that combines the magnetics and capacitors is developed. The integrated passive module can be used in resonant applications [79], non-resonant [80] applications, as well as used as EMI filters [81]-[83].

An integrated LC structure is proposed [84]-[86], shown in Fig. 17(a). The structure has a dielectric material sandwiched between two planar conductors, and a module having distrib-

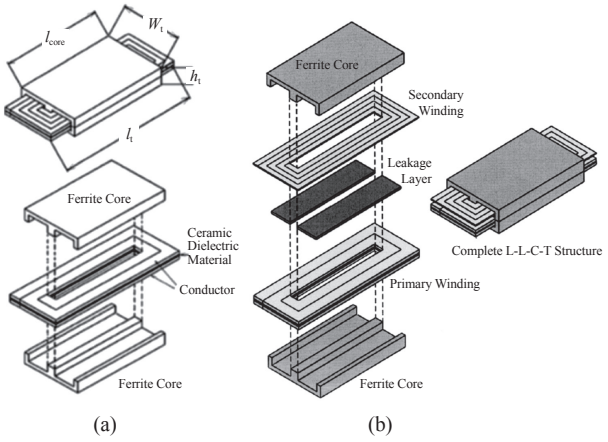


Fig. 17. Structure of LC and LLCT module [91].

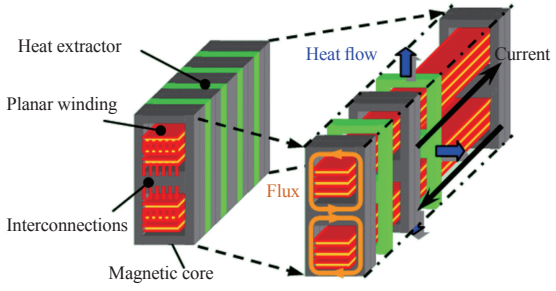


Fig. 18. Structure of heat extractor [99].

uted inductance and capacitance is formed. To further save space, capacitors, inductors and transformers are integrated together, forming the integrated LCT module [87]-[90]. For the resonant tank that contains magnetizing inductance, the structure of LLCT is obtained, shown in Fig. 17(b).

However, the optimized volume can't be achieved without accurate electromagnetic design and loss model. For the sake of the optimized design of the integrated module, electromagnetic model and design as well as loss calculation are developed [91]-[97]. Besides, to ensure the reliable operation, thermo-mechanical analysis is described in [98]. To further improve the power density without exceeding the highest temperature of material, a method for heat dissipation is essential. In [99], heat extractors are embedded into the magnetic core, shown in Fig. 18. A prototype that can achieve power density more than 1 kW/in^3 is obtained.

The LLCT modules have been implemented into resonant converter such as LLC resonant converter and non-resonant converter, namely asymmetrical half-bridge pulse width-modulation converter (AHBC) [44], [80], [100]. In [44], the LLC resonant tank is integrated into LLCT module, as shown in Fig. 19(a). The volume of passive integrated module is reduced to 14.6 cm^3. In [80], LLCT modules are implemented into current-doubler rectifier. To save the footprint, two LLCT modules are integrated into a single planar magnetic core, shown in Fig. 19(b). The total volume is 60 cm^3, which is much smaller than the discrete module. Therefore, by using LLCT module in the converter, the profile and volume can be decreased.

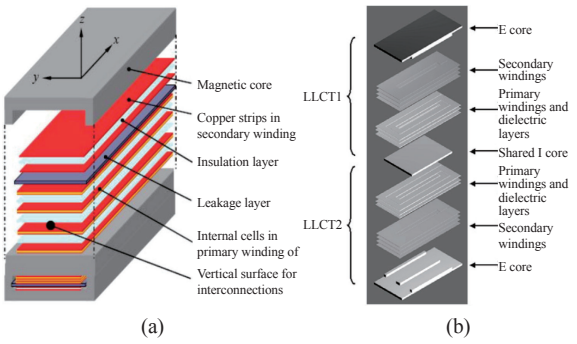


Fig. 19. (a) LLCL module structure of LLC converter [44]. (b) Current-doubler rectifier [80].

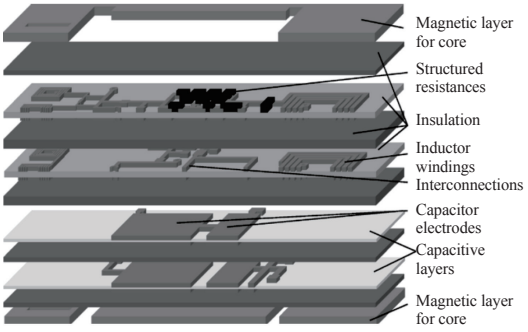


Fig. 20. Principle of emPIC proposed in [102].

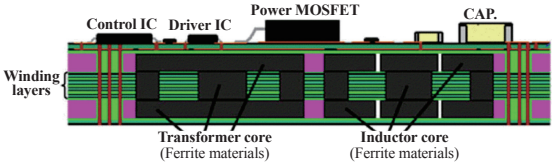


Fig. 21. Structure of emPIC proposed in [104].

To fully utilize the space and increase the heat dissipation ability, embedded passives integrated circuit (emPIC) is proposed [101]-[104]. In [102], capacitive layers and magnetic components are embedded in the PCB, shown in Fig. 20. The magnetic layers are achieved by utilizing ferrite polymer compounds named MagLam. In [104], a transformer and a inductor, using ferrite material having high permeability and low loss property, are integrated into PCB, shown in Fig. 21. An-eighth-brick with power density of 553 W/in^3 is obtained.

C. Power Supply on Chip and Power Supply in Package

A higher-level integration is to integrate the magnetic components with other components of the converter together, including the switches, drivers, and controllers. This kind of integration is possible to obtain a very high-power density, along with improved reliability and efficiency. At present, the technology is mainly used for low voltage and low power applications due to its complexity. The integration technology can be classified into two categories as PwrSiP and PwrSoC [105]-[107].

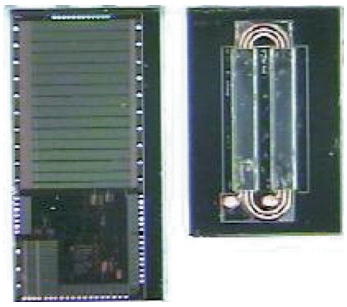


Fig. 22. A 20 MHz DC-DC converter IC and a 100 nH micro-inductor [108].

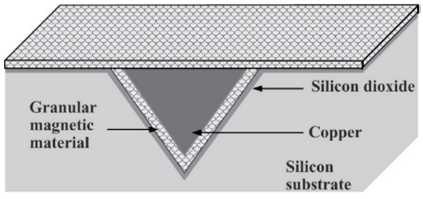
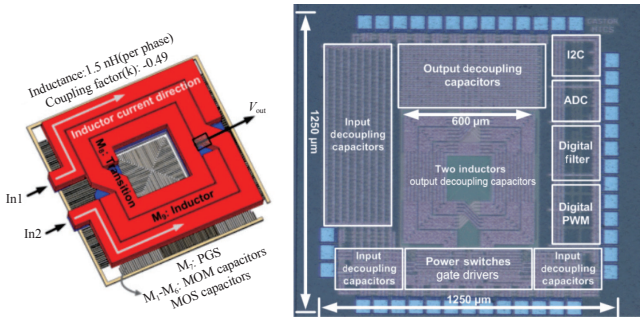


Fig. 23. Schematic of a V-groove inductor [110].



(a) (b)

Fig. 24. (a) Structure of a coupled air-core inductor. (b) Layout of the 500 MHz prototype IC [112].

PwrSoC is a wafer-level integration where the magnetic components are built in or on silicon die. A typical example is micro-inductor built on silicon for a 20 MHz DC-DC converter in Fig. 22 [108]. The coil is typically formed by depositing conductor on silicon wafers with a maximum thickness of 50 μm. The thickness of the magnetic material covering the coil is generally limited to within 10 μm. This inductor can only handle 500 mA of currents due to the limited coil thickness. R. Meere *et al*. builds a 100 MHz magnetic core inductor on silicon wafer, and it shows higher efficiency than a comparable air core inductor on silicon even at 100 MHz [109]. P. Dhagat *et al*. proposes a V-groove inductor to increase the current capability [110]. A V-shaped groove is formed on the silicon substrate by etching, as shown in Fig. 23. More copper materials can be deposited in the groove to form a thicker coil conductor, and as a result, this inductor can handle up to 7 A of current. More researches have conducted to further optimize this V-groove inductor [111]. Another typical example is the air-core inductor presented in [112]. The converter's operating frequency is pushed to 500 MHz, where the inductor needs only a very small value of 1.54 nH. This inductor was fabricated in a

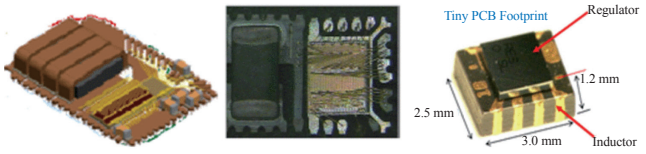


Fig. 25. Commercial PwrSiP products [107].

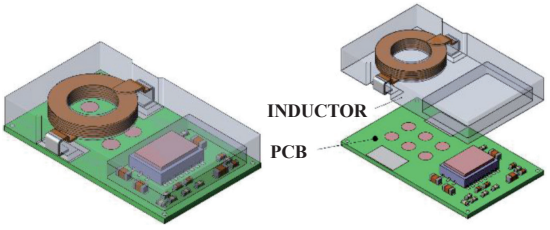
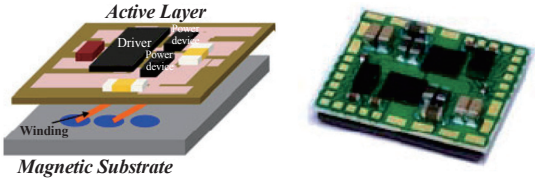


Fig. 26. Schematic of a power-system-in-inductor module [113].



(a) (b)

Fig. 27. 3D integration POL converter [115]. (a) Schematic. (b) Prototype of a two-phase interleaved converter.

65 nm CMOS chip. The output capacitor is also integrated into the chip. The total area occupied by the inductor and capacitor is only 1.1 mm^2, as shown in Fig. 24.

PwrSiP is to package a full converter into a single module, in which the magnetics and other components are connected internally. Compared to PwrSoC, PwrSiP is easier to be built and it can handle more power. Many companies have launched their own products [107], as shown in Fig. 25. To further improve the power density, many studies have been carried out. A power-system-in-inductor structure is proposed in [113], [114] where magnetic component is used as a package housing and the whole converter is packaged within the magnetic component, as shown in Fig. 26. Compared with the traditional plastic packaging structure, the inductor can gain much more space in the same package. As a result, the inductor can obtain greater inductance value and smaller DC resistance, which helps to improve the converter's efficiency. In addition, the thermal performance of the module can be improved because the thermal conductivity of the magnetic material is higher than that of the plastic material. Another typical example is the 3D integrated point of load (POL) converter proposed by CPES [115], [116]. Fig. 27 shows the concept of a 3D integrated POL converter. The active devices are soldered on the one side of the PCB or DBC substrate, and a low profile LTCC inductor is placed on the other side of the substrate. This module can operate at up to 5 MHz [117]. The power density of the 3D integrated POL converter can achieve a power density of as high as 1100 W/in^3, which is around 10 times higher than that of industry products at the same current level.

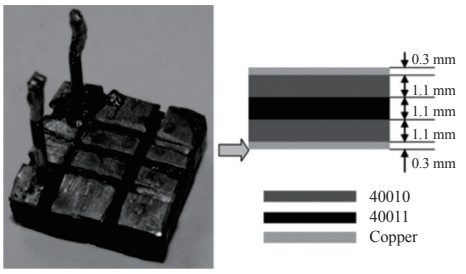


Fig. 28. Prototype of the nonlinear LTCC inductor [125].

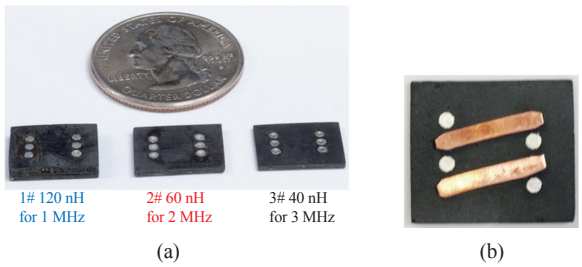


Fig. 29. LTCC inductors [129]. (a) LTCC cores at different frequencies. (b) Two phases coupled LTCC inductor.

D. LTCC Integration Technology

The LTCC material is made of ferrite tapes and ceramic tapes through stacking, pressing, co-firing and other steps [118]. It can be used to build passive components with low profile and flexible structure, which can help improve space utilization and facilitate integration [115], [119]. The CTE of LTCC material is around 5 ppm/°C, which is close that of silicon material, so that hybrid integration could be easily realized. The LTCC material also has higher thermal conductivity than FR4 used in PCB and thus features better thermal management.

An ultrathin coupled inductor based on LTCC technology was fabricated in [120], [121] for an interleaved buck converter. The thickness of the LTCC coupled inductor is only 1.3 mm. Another advantage of the LTCC inductor is that it has a distributed air gap, which is beneficial to reduce the AC loss of the winding when compared with the traditional air gap inductor. However, the flux density distribution of the distributed air-gap LTCC inductor is not uniform in the magnetic cores, which can cause the magnetic core near the conductor to saturate easily while the core away from the conductor is not fully utilized. To address this problem, Wang *et al*. [122]-[124] proposes a multi-permeability distributed air-gap magnetic structure. The internal permeability is lower than the external permeability, so a more uniform magnetic flux density distribution can be obtained. The multi-permeability LTCC inductor can achieve higher inductance value and relatively stable inductance value than the single permeability LTCC inductor without increasing the inductor size. A nonlinear LTCC inductor is proposed in [125]-[127]. The core of the LTCC inductor is made of ferrite tapes with different permeability. As the DC current increases, the ferrite tapes with high permeability gradually saturates, causing the inductance to drop gradually. This nonlinear inductor has a relatively large light-load inductance, which can help reduce light-load current ripple and thus improve the light-load efficiency. Fig. 28 shows a prototype of the nonlinear LTCC inductor with two different permeability.

CPES has conducted a series of studies for 3D POL integration using the low profile LTCC inductors as a substrate [128]-[136]. The use of low profile inductors allows for more efficient use of space when integrated with the active devices. Fig. 29 shows the LTCC inductors substrate. As the frequency increases, the LTCC inductor can be made thinner, thereby increasing the power density. To obtain a better performance of the LTCC inductor substrate, some studies have been carried out. The characteristtics of the LTCC ferrite tape is explored detailly in [137]. Li *et al*. [136] proposed several models to calculate inductance for the LTCC inductor. A numerical model is proposed in [138] and an analytical model is proposed in [139] to calculate the core loss. Based on these studies, the LTCC inductor substrate is fully optimized for 3D integrated POL converter. Along with the layout optimization to reduce parasitic inductance, the use of DBC substrate to enhance heat dissipation, and the use of GaN devices to reduce switching losses, the switching frequency of the 3D integrated POL converter is pushed up to 5MHz [117]. Furthermore, a two phase LTCC coupled inductor is designed for the 3-D integrated POL converter, in which the frequency of the AC magnetic flux of the LTCC inductor reaches 10 MHz. The core thickness of the LTCC coupled inductor is only 0.4 mm.

IV. Conclusions

This paper reviews the state-of-the-art integration technologies involving active and passive integrations. The active integration technologies are reviewed from the aspects of interconnection technology, packaging material technology, packaging structure technology, and module-level integration technology. The emergence of wide band-gap semiconductor devices puts forward higher requirements for active integration technologies, especially parasitic and cooling issues. Great advancements have been made in active integration technologies. 1) Advanced wirebond-less technologies and advanced packaging structures (including 2.5D structures and 3D structures) have been developed to realize small parasitics and high heat-dissipation capability; 2) Emerging die-attaching materials, such as nano-silver sintering and TLPB, have demonstrated excellent high-temperature performance, and are promising for high power density applications; 3) The modules with integrated gate driver, decoupling capacitor, sensors, and heat sinks, etc. have been developed to achieve better performance. The passive integration technologies are reviewed from the aspects of the magnetic integration technology, electromagnetic integration technology, PwrSoC and PwrSiP technology, and LTCC integration technology. Magnetic integration technology and electromagnetic integration technology can effectively reduce the size of passive components, and have been applied to the various circuits, such as current-doubler rectifier, multiphase

converter, LLC converter, etc. PwrSoC is a wafer-level integration and suitable for low current (below several amps) applications, while PwrSiP can handle currents up to 40 A. CPES has successfully developed a 3D integrated module with power density up to 1100 W/in^3. The LTCC magnetics have been successfully applied to high-frequency high-current 3D integrated module, and are expected to be extended to higher power integrated modules.

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Empowering the Electronics Industry: A Power Technology Roadmap

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***Abstract*—The Power Sources Manufacturers Association (PSMA) currently publishes an updated Power Technology Roadmap (PTR) every two years. This paper describes the methodology used and the key findings captured in the tenth edition which was published in March 2017. Applications driving the roadmap needs are presented along with the direction of technology advancement in components, power supplies and converters. Emerging technologies which promise the potential of further advancement, but are not yet proven, are also discussed.**

***Index Terms*—Emerging technologies, power technology, PSMA, PTR, roadmap.**

I. Introduction

THE Power Technology Roadmap (PTR) published by the Power Sources Manufacturers Association (PSMA) helps align the power electronics industry by tying together the needs and direction of a broad range of stakeholders.

The latest roadmap document published in 2017 exceeds 500 pages [1]. This paper merely provides a summary of how the roadmap is assembled and offers a flavor of the type of content that is included.

The purpose of the PSMA, a not-for-profit organization, is to enhance the stature and reputation of its members and their products; improve their knowledge of technological and other developments related to power sources; and educate the electronics industry, academia, and government and industry agencies as to the importance of, and relevant applications for, all types of power sources and conversion devices. The membership ranges from Original Equipment Manufacturers (OEMs) who use and specify power conversion equipment, through manufacturers of power supplies and converters, to component manufacturers of active and passive devices. The membership also includes individuals involved in power electronics consulting and institutions involved in academic and pre-commercial research and development in the area.

To support the purpose of improving knowledge of technological and other developments related to power sources, a PTR committee is sponsored with the purpose of regularly publishing a roadmap document to help guide and align the members and other stakeholders. The roadmap document is currently published every two years and this paper reviews the methodology and contents of the tenth edition published in March 2017.

Fig. 1. Power technology roadmap cube.

While some enhancements in gathering and presenting data are being considered for the eleventh edition, the committee envisions that the basic format of the tenth edition will carry into the next edition.

II. Methodology

In March 2015, in conjunction with the APEC conference, the PSMA PTR committee held a kick-off meeting to review the scope of the report. There was also a lessons-learned analysis of the just released PTR 2015 report to facilitate learnings and improvements. Like the previous roadmap, the report's structure remained a three-dimension overview of:

- Power Supply & Converter products and technology (ac-dc front-end power supplies, external ac-dc supplies, isolated and non-isolated dc-dc converters)
- Components Technologies (power semiconductors, ICs, magnetic materials, etc.)
- Applications and Emerging Technology Trends (which may be used across many products and are enabled by many components)

Fig. 1 provides a 3D visualization of the power technology roadmap structure. The power technology roadmap cube ("PTR Cube") shows how each of the technology, component, and application segments intersect and overlap, describing the dependency between multiple cross segments.

A dedicated segment to address the component facet of the

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PTR cube was introduced in the 2017 PTR report. In earlier roadmaps, this facet was largely addressed through the webinar coverage.

To gather data from a broad range of experts, a series of webinars were conducted between January 2016 and February 2017. The webinars covered a wide range of power conversion topics loosely grouped into Application Trends, Component Technologies, Emerging Technologies and Power Supply & Converter Trends. These presentations are listed below:

Application Trends

- Synergies Between Power Electronics and Energy Harvesting
- An Overview of Wireless Power Transfer and Standards
- Power and Sensor Devices Driving Automotive Semiconductor Applications
- iNEMI 2017 Energy Storage Roadmap—A Summary Component Technologies
- Trends in High-Frequency Magnetics and Power Supply Design
- Wide Bandgap Power Devices: Die Size Shrinking and Its Impact on Power Delivery Architecture
- GaN Power ICs and the High Frequency Eco-System
- SiC Power MOSFETs and Applications Status in 2016
- Technology Trends and Advances in Multilayer Chip Ceramic (MLCC) and Metallized Polypropylene Film Capacitors

Emerging Technologies

- Significant Developments and Trends in 3D Packaging with Focus on Embedded Substrate Technologies
- Nanofluids for Electronic Cooling

Power Supply and Converter Trends

- Present and Projected Safety-Regulatory and Compliance Requirements for Power Conversion and Power Supplies
- It's all about the insulation—Choosing the best digital isolator

The presentations were from OEMs, suppliers, technologists, research labs, and academics. These presented snapshots of today's state-of-the-art in power conversion technology, what the end customers are expecting in the next few years, and how the component technology is changing.

The webinars, including the question and answer segments, were recorded to allow the segment teams to review the presentations for estimating trends for each product. The recorded material is available as part of the electronic copy of the roadmap report. The webinars add much to the presentation materials as the listener can hear and understand the context and the subtext of the original presentation in the speaker's voice.

For the second part of the roadmap process, the core team and the volunteers divided into four segment teams. Each team is responsible for a different type of product (Power Supply and Converter Technology), chosen as representatives of the overall market:

- Ac-dc front-end power supplies (200 W–2000 W)
- External ac-dc power supplies (10 W–100 W)
- Isolated dc-dc converters (100 W, regulated)
- Non-isolated dc-dc converters (sub-divided into the standard non-isolated dc-dc and power supply in a package (PSiP) converters)

For each, the group made their best assessments of the technologies and metrics to track. A significant effort was made to streamline the survey questions (for both the online survey and the more detailed trends tables) to allow ease of data entry.

The online survey was created and sent out to the PSMA mailing list for responses. After the online survey closed, each segment team examined the results as they applied to their focused power supply design segment. Conference calls and questionnaires were used to gather inputs from other stakeholders. The consolidated results were then captured in a series of defined tables, which formed the basis of the trend tables. These tables convey the main quantitative substance of the report.

In the third part of the roadmap process, the application and technology commentaries provide windows into understanding key issues of the end applications and important technologies. Various industry leaders contributed articles on the general trends, key metrics, key market drivers, and challenges of each application segment. TABLE I lists the covered areas for applications, component technologies and emerging technologies.

TABLE I
APPLICATION AND TECHNOLOGY COVERAGE

Application Segments	Component Technologies	Emerging Technologies
Automotive	PWM Controllers	Magnetics
Computing	Low and Mid	Integrated
Consumer	Voltage MOSFETs	Magnetics
Lighting	IGBTs	3D Power
Medical	High Voltage	Packaging
Motor Control	MOSFETs and GaN HEMTs	Additive
Portable Charging	SiC Devices	Manufacturing
Energy Harvesting	Passive Components	Nanofluids

III. APPLICATIONS

Power Electronics, like any other technology, is responsive to the needs of end applications in which it is embedded. Since power technology in one form or other is an integral part of any electronic system, the applications range for power technology is very diverse. In this section, the trends in end applications and their impact on power technology are covered.

The application trend overviews are written by a diverse group of experts representing power supply manufacturers, semiconductor manufacturers and research institutes. Experts were provided a simple template to express their views but were also encouraged to forge their own path and modify as they deemed necessary. The application segment overviews are intended to complement more in-depth and focused information found in the other sections of the PTR report. Topics that are covered include: automotive, computing, consumer, lighting, medical, motor control, and portable charging. This year energy harvesting segment made a debut keeping up with changing trends in power electronics.

TABLE II
AUTOMOTIVE SAFETY FEATURES

Active Safety	Passive Safety
Anti-Lock Brakes	Seat Belts
Traction Control	Air Bags
Active Suspension and Electronic Stability Control	Collapsible Steering Column
Lane Departure Warning/Lane Assist	Passenger Compartment Crumple Zones
Emergency Brake Assist/Collision Avoidance	Head Impact
Pedestrian Avoidance	

The template followed by all the contributors includes the following sections:

- Introduction—A high level introduction to (or overview of) the application segment.
- Marker Drivers—Identification of two to three key application areas that are having largest impact on the whole segment and the implications for power electronics.
- Key Metrics—Identification of important power electronics metrics or specifications and how they are driving power electronics evolution for the segment.
- Trends—Identification of end use trends or disruptive forces that impact the application segment.
- Challenges—Discussion of the biggest challenges for power electronics industry and its components in the applications segment.

A. Automotive Applications

Worldwide initiatives to reduce emissions and improve active and passive safety (as shown in TABLE II) were identified as key market drivers. Lower battery costs, higher consumer acceptance and wider availability of charging infrastructure are the factors driving growth in electrical vehicle adaption. Driver comfort and convenience features for infotainment, lighting and connectivity are also driving power electronics growth in automotive field.

Choice of voltage rails, EMI standards and standby power drain were some of the key metrics identified. Key trends included enhanced safety features such as automatic braking, enhanced illumination and lighting, move to higher voltage rails and increased efficiency. EMI immunity and controlling emissions as the systems get more complex was the major challenge identified.

B. Computing Applications

For the datacenter market, hyperscale and hyperconvergence are identified as the overarching trends. Energy efficiency improvement, lower power consumption and use of standardized hardware are the key market drivers for power technologies. Power Usage Effectiveness (PUE) and its reciprocal Data Center Infrastructure Efficiency (DCIE) remain the key metrics.

TABLE III
EUROPEAN COC ACTIVE MODE EFFICIENCY CRITERIA

Rated Output Power (P_{no})	Minimum Efficiency in Active Mode at 10% load of full rated output current	
	Tier 1	Tier 2
$0.3 < W < 1$	$\geq 0.500 * P_{no} + 0.046$	$\geq 0.500 * P_{no} + 0.060$
$1 < W < 49$	$\geq 0.0626*\ln(P_{no}) + 0.546$	$\geq 0.071*\ln(P_{no}) - 0.00115 * P_{no} + 0.570$
$49 < W < 250$	≥ 0.790	≥ 0.790

The growth in hyperscale architectures is creating a trend away from proprietary hardware. Also, growth in the storage market has highlighted the need for capacity and speed. Achieving the right balance between the cost and performance remains the primary challenge for computing power technologies.

C. Consumer Applications

The consumer applications commentary focused on USB-PD Type-C connector and its impact on charging of consumer devices such as smartphones, tablets and Notebook PCs. The market drivers are quick-charging technologies, higher power level requirements and need for universal compatibility. Key metrics are the regulatory requirements for active mode efficiency and no-load power.

The main trends in this area are migration to type-C connector for USB Power Delivery at higher power levels and corresponding need for new topologies that lead to higher power density of travel adapters. Efficiency performance of the ac-dc converters (as listed in TABLE III), and consolidation of the quick-charging technologies remain the key challenges.

D. Energy Harvesting

Examples of different energy harvesting sources are shown in Fig. 2.

The need for low power IoT devices to become self-powered or extend their battery life using energy harvesting is addressed. The explosive growth in IoT devices and the concerns about their availability due to battery life are the key market drivers for energy harvesting. Need for new metrics at system level in this emerging area is highlighted. One of those is defining behavior of power conversion circuits at very light and sporadic loads.

Trends in various sub-segments such as transducers, storage devices, PMICs, Magnetics, Capacitors and Low power sensing and processing are identified. Key challenges for energy harvesting are: limited and sporadic availability of ambient energy, need for miniaturization and related packaging challenges, and system level optimization.

E. LED Lighting Applications

LED lighting applications continue their penetration per Fig. 3. Applications covered include (a) retrofit residential, (b) ret-

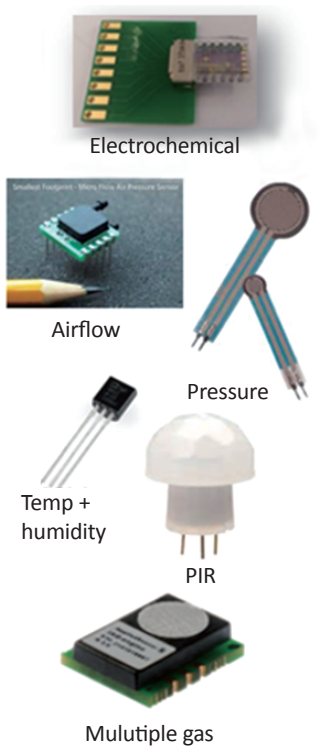

Fig. 2. Examples of energy harvesting sources.

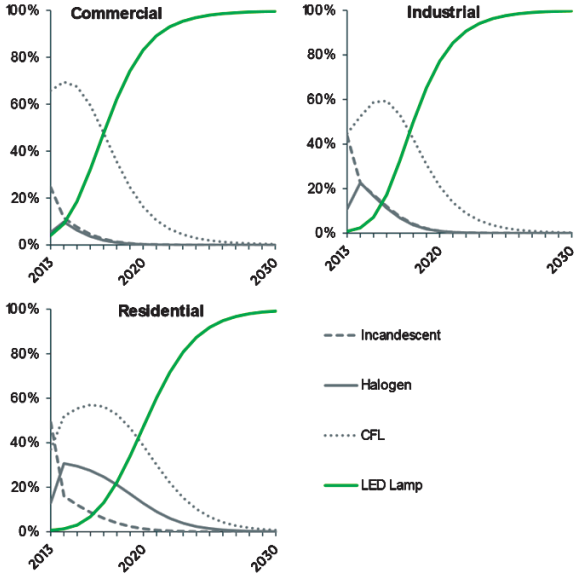

Fig. 3. Projected growth in LED lighting market-share (Source: US DoE, August 2014).

rofit industrial/commercial and (c) new constructions. Cost is a market driver for (a) and (c), while ease of installation is the driver for (a) and (b) and performance is the driver for (b) and (c). Some of the key metrics include operating life/reliability, compatibility, standby power, efficiency, THD/PF, and quality of light.

Key trends include selective transition from isolated to non-isolated LED drivers, single-stage topologies, selective use of PFC front-end, lower component count and deeper dimming. Some

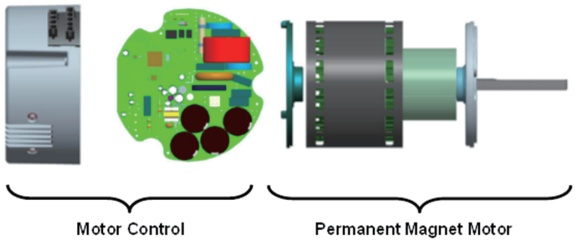

Fig. 4. Typical residential HVAC integrated motor drive.

of the challenges include flicker reduction and lower acoustic noise and compatibility for T-lamp replacement.

F. Medical Applications

The drivers for growth of power electronics in medical applications are identified as the aging population and advances in medical electronics to serve their healthcare needs. In addition, more stringent compliance standards are also expected to shape the evolution of medical power electronics.

Development of artificial intelligence, deep learning and machine learning; 3D medical printing; and growing popularity of surgical robotics are some of the major trends. The challenges include the trade-offs between needs for higher density and safety requirements; changes in EMC as legislated by IEC60601-1-2; reducing development costs while meeting safety and regulatory regime; and improving active mode and standby efficiency of home healthcare devices as they proliferate further.

G. Motor Control

The need for high-efficiency motor drive systems is highlighted given their total share (~40%) of world-wide energy consumption. An example is shown in Fig. 4. The drivers include need for efficient variable speed control, optimized performance for a given application and cost reductions.

Key trends include higher level of electronic component integration and sophistication of software to simplify hardware and give more options to consumers, including connectivity. Major challenges include thermal management with higher power density and component life/reliability with more constrained environments.

H. Portable Charging

Portable charging of single-cell (low and high power) and multi-cell Li-ion batteries is covered. The main drivers are high-current charging and universal charge compatibility, with USB Power Deliver gaining traction across multiple power levels per the example of Fig. 5. Additional driver is the proliferation of other mobile devices. Key metrics include energy density, cost, temperature capability, and reliability.

The trends in portable charging consist of high input voltage chargers; incremental converter efficiency improvements; parallel chargers; low-voltage, high-current chargers; and buck-boost architecture for universal compatibility of multi-cell chargers. The main challenge is in effectively addressing the end

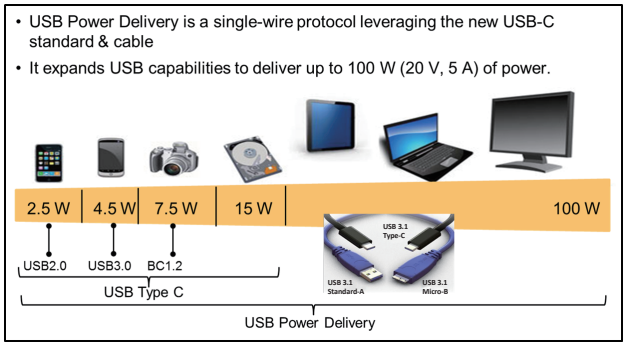

Fig. 5. USB power levels.

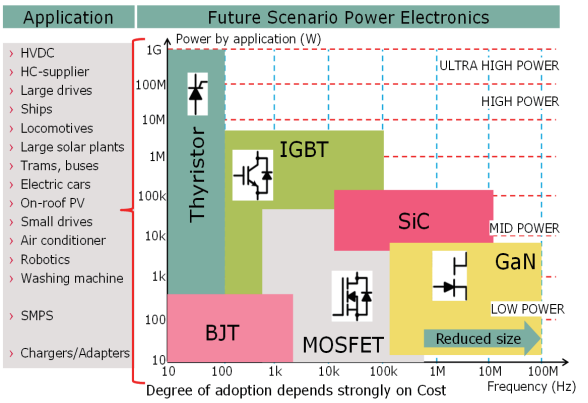

Fig. 6. Switching power device application space.

consumer's battery life anxiety, while providing ever-growing functionality. Adding intelligence and flexibility while increasing the charge current and reducing the temperature is another significant challenge.

IV. Components

High-frequency, switch-mode, power-conversion equipment functions by controlling the flow of energy in discrete time intervals. This requires components and devices that store that energy along with components and devices that allow the energy to flow from one part of the circuit to another at the appropriate time. Magnetic and capacitive devices are the primary energy storage technologies (batteries are not addressed in this section). Semiconductor switches and controllers control the energy flow.

Incremental, and occasionally significant, improvements in components and devices continue to enable the ever-increasing density and efficiencies of power conversion equipment. The industry may be on the cusp of another step change as wide band gap (WBG) semiconductor switches become commercialized. These devices offer the potential of much higher switching frequencies, and therefore density, while maintaining or even improving efficiencies. These potential improvements are not without their challenges, and impact all components, including the semiconductor switches, the energy storage devices and the controllers.

A. Wide Bandgap (WBG) Technology Trends

For power technology applications, the two applicable WBG devices are Gallium Nitride (GaN) and Silicon Carbide (SiC) switches. Fig. 6 illustrates the frequency/power level space these new devices are carving out in various applications.

1) GaN Devices

The GaN power switches are relatively new and are getting utilized in niche applications such as datacenter power and specialty high efficiency adapters. By reducing switching losses significantly, GaN switches improve efficiency and enable higher power density conversion. Another highlighted benefit of GaN devices is low and linear output capacitance, which enables shorter dead-time in ZVS applications—leading to higher available duty cycle and lower rms currents and/or higher frequency operation.

Performance of GaN switches is measured by 3 Figures of Merit (FOM) shown below. In all of the FOM, GaN shows superior performance to Silicon Superjunction FETs.

- $R_{DS(ON)}$ x Qoss–about 10x improvement
- $R_{DS(ON)}$ x Qrr–about 10x–100x better
- $R_{DS(ON)}$ x Qg–about 12x improvement

Identifying and employing topologies that take advantage of these FOMs is key to rapid adaptation of GaN devices in mid-high power applications.

The major challenges for GaN devices include cost and reliability. While cost projections indicate rapid drop as volumes increase, the reliability issue is being addressed by industry-wide standards development groups.

2) SiC Devices

Compared to GaN devices, SiC devices have been around longer, but the SiC MOSFET has gained maturity and wider acceptance in recent years. Most of the offerings are planar DMOSFETs, with some trench device availability. The market drivers for SiC adaption are the need for higher power density and (often) lower cost due to high switching frequency operation.

SiC devices are typically used for 1200 V applications, though some lower voltage (650 V and 900 V) applications are also starting to use SiC devices. One of the trends is reduction in specific $R_{DS(ON)}$ of the devices—which is in the range of 2.5 $m\Omega \cdot cm^2$—significantly lower than Silicon.

While the market drivers for SiC remain strong (due to growth in Electric Vehicles and Renewable Energy power conversion), the key challenge remains the device cost. Also, the end users' lack of familiarity with high frequency designs or other practical issues such as EMI concerns could limit the growth of the SiC devices.

B. Passive Component Trends for High Frequency

Improvements in WBG devices are also accompanied by improvements in magnetic and capacitors while setting new challenges for those same device technologies.

Some of the improvements are captured in depth in Section VI below. Others are discussed, and will continue to be discussed in industry workshops organized by the PSMA. Topics such as core materials, characterization and modeling under

realistic circuit operation has been covered in the 2016 [2] and 2017 workshops [3]. Two workshops are also planned for March 2018 in conjunction with the APEC 2018 conference; one will address magnetics winding losses [4] while the other will address capacitor technologies [5].

Space does not permit detailed discussion of these topics in this paper. Instead readers are encouraged to contact the PSMA committees responsible for the workshops for further information.

V. Power Supply and Converter Trends

The roadmap tracks four power supply and converter product segments. These segments are unchanged from recent reports, which facilitates reporting on long term trends. One of the segments, ac-dc front-end power supplies, can be traced back to the original roadmap in 1994. The scope of the dc-dc segments has evolved over time. External ac-dc power supplies were added later.

These tables convey the main quantitative substance of the report.

A. Ac-Dc Front-End Power Supplies

This segment covers ac-dc power supply technology from 200 W to 2000 W. While computer servers tend to drive many of the technological advancements, the questions are structured to gain a view beyond front-end power supplies for servers and include perspective on trends in telecom, industrial and medical applications.

The survey only considers power supplies with a single, main output, usually in the range of 12 V to 48 V. The power supplies in question:

- Will typically be enclosed in a metal box at higher power level, but may be open frame in power levels closer to the 200 W lower limit;
- Can be hot-swapped, pluggable designs or fixed-chassis-mount in style;
- Can have an internal fan, especially at higher power levels, but may also be system cooled. Convection ratings are possible at the lower power levels and as efficiency levels increase, but the majority of power supplies in this range are still cooled by moving air.

Because the power range is broad, some questions have been split in two to separately address the 200–600 W and 600–2000 W spaces.

1) General Observations

Some disparate opinions on priorities for Telco applications were noted with some contention between the relative importance of cost and reliability in a rapidly changing, yet highly competitive industry.

The emergence of 380 Vdc, and similar, high voltage distribution in high-end computing and telecommunications environments was noted in prior roadmaps and continues to be mentioned in the surveys. However, adoption to date has remained low.

TABLE IV
Ac-Dc Front-End Trends (General)

Parameter/Metric	2019 Est. (PTR 2015)	2017	2019	2021
Peak Efficiency @ 48 V Output at any load (Eff%)				
Most Economical Models	94.0%	95.5%	95.5%	96.0%
Highest Practical Models	96.5%	96.5%	96.5%	97.0%
Leading Edge Models	97.5%	97.3%	97.5%	98.0%
Peak Efficiency @ 12 V Output at any load (Eff%)				
Most Economical Models	93.0%	93.5%	94.0%	94.0%
Highest Practical Models	96.5%	96.0%	96.1%	96.3%
Leading Edge Models	97.0%	96.3%	96.3%	96.5%
Efficiency Profile vs. Load				
Flat efficiency profile over load range	40%	30%	32%	35%
Efficiency Optimized for Half-Load	30%	45%	43%	40%
Efficiency Optimized for Full-Load	10%	15%	15%	15%
Don't Care	20%	10%	10%	10%
	100%	**100%**	**100%**	**100%**
Power Management Interface Technology (%)				
No Power Management Interface	10%	8%	6%	4%
Discrete Digital and Analog Signals Only	15%	15%	12%	10%
Serial Bus Interface Only	40%	37%	42%	48%
Mix of Discrete Signals and Serial Communication Bus	35%	40%	40%	38%
	100%	**100%**	**100%**	**100%**

277 Vac and 480 Vac operation continues to be a bigger factor, expanding beyond LED drivers to Datacenters and other applications.

Efficiency levels continue to trend upwards but at a slower rate as other system level approaches are utilized for energy conservation.

Power Factor Correction (PFC) switching frequencies remain relatively low, typically below 150 kHz. But commercialization of GaN offers the potential to increase the frequency where the higher component cost can be managed.

LLC converters continue to gain share in the Dc-Dc section of the power supply, and switching frequencies may also trend upward here as GaN becomes suitable.

The momentum behind the adoption of digital and mixed-signal controllers continues unabated for both PFC and Dc-Dc stages.

2) Trend Tables

The entirety of the report and this segment is written by experts in the field, thereby bringing value to the power conversion community. However, much of the report is qualitative and many come to the report seeking quantitative assessment. TABLE IV and TABLE V in this section provide examples of that insight. Space permits only limited examples and the reader is referred to the full report for more detail.

TABLE V
AC-DC FRONT-END TRENDS (DC-DC STAGE)

Parameter/Metric	2019 Est. (PTR 2015)	2017	2019	2021
Primary Switch Technology (%)				
Silicon MOSFET (including SuperJunction)	83%	90%	83%	70%
Silicon Carbide FET	5%	3%	5%	14%
IGBT	0%	1%	0%	0%
GaN FET	10%	5%	11%	15%
Other (e.g. GaAs FET)	2%	1%	1%	1%
	100%	**100%**	**100%**	**100%**
Transformer Winding Technology (%)				
Traditional Wire And Foil Wound On A Bobbin (Primary & Secondary)	25%	25%	20%	18%
At Least One Flat Or Planar Winding Of Any Construction Or Material	75%	75%	80%	82%
	100%	**100%**	**100%**	**100%**
Inductor Winding Technology (%)				
Traditional Wire And Foil Wound On A Bobbin	65%	65%	50%	45%
At Least One Flat Or Planar Winding Of Any Construction Or Material	30%	30%	40%	40%
Topology requires no separate output inductor	5%	5%	10%	15%
	100%	**100%**	**100%**	**100%**

TABLE VI
AC-DC EXTERNAL TRENDS

Parameter/Metric	2019 Est. (PTR 2015)	2017	2019	2021
Output connector (%) (<15 W)				
Permanent Cable		29%	21%	17%
USB Type A		17%	17%	15%
USB Type B		16%	18%	17%
USB Type C		17%	23%	29%
Other		22%	22%	22%
		100%	**100%**	**100%**
Output connector (%) (15–65 W)				
Permanent Cable		43%	42%	33%
USB Type A		10%	6%	4%
USB Type B		12%	10%	8%
USB Type C		6%	20%	42%
Other		30%	22%	14%
		100%	**100%**	**100%**
Peak Efficiency – (<30 W Models) (Eff%)				
Most Economical	79%	76%	79%	79%
Highest Practical	88%	88%	88%	88%
Leading Edge	93%	92%	93%	95%
Peak Efficiency – (30–100 W Models) (Eff%)				
Most Economical	86%	85%	86%	87%
Highest Practical	91%	90%	91%	92%
Leading Edge	94%	93%	94%	95%
No Load Power Consumption (mW)				
Most Economical	150	200	150	90
Lowest Practical	30	30	30	20
Leading Edge	5	10	5	5

B. Ac-Dc External Power Supplies

External ac-dc power supplies are commonly known as ac adapters. They are widely used for consumer and mobile products; including cell phones, tablets, laptop computers, portable DVD players, set-top boxes, printers, display monitors, and smaller flat-screen televisions. The advantages include weight and size reduction of the main product, safety (due to keeping the mains voltage out of the end product and electrically isolating it), reducing EMI problems within the product, and allowing multiple sources for the adapters. Along with the advances in technology of the end products, there have been consistent improvements in the technology of the ac adapters themselves fueled by end-user demands for smaller, more efficient, and more reliable products and by regulatory agencies worldwide in their pursuit of energy conservation. Due to the consumer nature of adapters, the trends' adoption rate has been tempered by the need to keep the total cost of new solutions nearly the same as existing solutions.

1) General Observations

The power levels of phone chargers are increasing driven by the higher capacity batteries and the need for fast charging. At the same time, laptops are becoming more energy efficient and power levels in these applications are stable, or even falling.

Flybacks remain the topology of choice below 100 W, but spread across hard-switching, quasi-resonant and active clamp variants. Above 100 W, LLC topologies are gaining momentum.

As power levels increase, integration of active devices is increasing to improve power density. GaN- and SiC-based solutions are being pursued in this area but have not yet been broadly adopted as costs continue to be addressed.

2) Trend Tables

TABLE VI provides an example and readers are recommended to view the entire report for additional quantitative data.

C. Isolated Dc-Dc Converters

Demand for isolated dc-dc converter modules continues to be dominated by applications in the converged computing and telecommunications market segment as the integration of voice and data communication capabilities into the internet backbone is almost complete and in a steep commoditization trend. Data center applications require system-level solutions that optimize size and efficiency and are driving the proliferation of digital interface control and real-time adaptability of the various versions of the intermediate bus architecture. Industrial, military,

aerospace, and other applications remain significantly smaller, yet still drive industry segmentation with parameters like input voltage range, packaging, and environmental requirements.

While the power levels can vary broadly, the parameters captured in this survey focus on 100 W isolated converters to allow consistent trend-tracking from year to year. These trends are believed to be reasonably representative and can be scaled to the broader space.

1) General Observations

Converter packages are expected to continue to shrink, with the market tilting in favor of smaller packages. In the next five years, no single package size will be dominant; buyers will find more options at the same power level, but with a wide variety of features and functionality.

More command and control ability is added to existing sizes to increase value at existing power densities.

Soft switching topologies and fixed-frequency designs are expected to dominate the converter market in 2019 as manufactures leverage advancements in FET technologies and increasing levels of device integration.

The demand for high voltage (270 or 380 V input) converters by 2019–2021 is expected to noticeably increase due to multiple market segments leveraging the inherent benefits of HVDC distribution architectures. The traditional (wide) telecom input range continues to be popular and widely used.

2) Trend Tables

TABLE VII provides an example and readers are recommended to view the entire report for additional quantitative data.

TABLE VII
ISOLATED DC-DC TRENDS

Parameter/Metric	2019 Est. (PTR 2015)	2017	2019	2021
Input Voltage Range (%)				
Telecomm Wide Range (36–75 V, 36–72 V, etc.)	35%	56%	45%	30%
Narrow Range (48 V ±5% Or +5% /–10%)	32%	28%	32%	29%
24 or 28	9%	11%	10%	12%
270 or 380	23%	5%	13%	29%
		100%	**100%**	**100%**
Expected Maximum Output Current (A)				
Quarter Brick	135	64	76	89
Eighth Brick	83	37	44	53
Sixteenth Brick	49	17	21	26
Expected Efficiency–most advanced (Eff%)				
48Vin - 3.3Vout (regulated)	94%	88%	89%	91%
48Vin - 12Vout (regulated)	96%	92%	94%	97%
48Vin - 12Vout (unregulated)	98%	92%	95%	95%
380Vin - 12Vout (regulated)	97%	92%	96%	96%
380Vin - 12Vout (unregulated)	98%	92%	96%	96%
Power Management Interface Technology (%)				
None	30%	51%	44%	37%
I2C	27%	13%	20%	23%
PMBus	39%	16%	30%	40%
Other	4%	20%	6%	0%
		100%	**100%**	**100%**

D. Non-Isolated Dc-Dc Converters

Non-isolated dc-dc power converters make up one of the largest segments in power conversion architecture. The converters are used in server, networking, telecom, industrial, consumer, and automotive applications for powering the intermediate bus and/or final applications where low voltage and higher current loads are used. For safety reasons, non-isolated converters almost universally have a maximum input voltage of less than 100 V. Telecom, networking, and industrial applications have input voltages more in the 12 V to 48 V range. The output voltage is typically at or below 5 V. Exceptions are sensors, analog IC loads, specialty and motor control, or emerging applications with output voltages as high as 12 V or applications that require negative voltage. In most applications where non-isolated dc-dc converters are used, the digital loads are CPU, GPU, memory chips, DSP, FPGA, and ASICs that require fast transient response with minimal voltage deviation. These lower voltage converters have outputs in the range of 0.5 V to 2.5 V with load currents varying from a few amps to hundreds of amps. These are the last stages in the power conversion process and define the term point of load (POL).

1) General Observations

Output voltages provided by non-isolated converters continue to drop about 50 mV per year while the load currents and power are increasing about 10% per year. As the trend tables and survey results show, many high-end boards now have power rails down to 0.5 V.

After EMI, the survey respondents selected power density as the most important feature, followed by efficiency. Even though power density is in the top design criteria, the switching frequencies are predicted to remain stable at 600 kHz to 2 MHz.

The number of PCB layers for a typical non-isolated converter design is increasing, with six or more layers becoming the dominant construction of most converters. Meanwhile, the number of PCB layers on discrete converter/ regulator on server boards has reached the twenties. To save space, most regulators have switched to non-standard QFN packages, with large areas under the package to remove heat and carry large load currents. For currents lower than 20 A, Power Supply in a Package (PSiP) and Power Supply on a Chip (PwrSoC) packaging technologies are considered cost-effective alternatives to the modules.

Although many respondents predict digital implementation of the control loop proliferating in the next five years, they still think a large majority of converters (>60%) will continue using pure analog feedback control.

There is a strong interest in 48 V POL conversion, especially for high-power CPU/GPU type loads. As the high-end server power requirement per board is increasing, distribution losses with traditional 12 V architecture hurt efficiency.

TABLE VIII
NON-ISOLATED DC-DC TRENDS

Parameter/Metric	2017 Est. (PTR 2015)	2017	2019	2021
Input Voltage Range (Vin) (% of Total Market)				
Above 14 V and below 54 V	4.0%	6.0%	6.3%	6.5%
Wide Range (3 V < Vin < 13.2 V)	35.7%	25.0%	24.5%	24.0%
12 V Narrow (10.8 V < Vin < 13.2 V)	27.7%	27.5%	27.3%	27.0%
10–12 V Wide (7.5 V < Vin < 13.2 V)	18.0%	29.0%	29.8%	30.5%
3.3–5 V (3 V < Vin < 6 V)	13.7%	11.5%	11.3%	10.5%
Other	1.0%	1.0%	1.0%	1.5%
	100%	**100%**	**100%**	**100%**
Peak Efficiency (Typical Peak) (Vin = 12 V, Vout = 1.2 V, Iout = 60 A) (Eff%)				
Most Economical	86.7%	86.8%	87.3%	88.3%
Highest Practical Performance	92.3%	90.8%	91.3%	92.3%
Leading Edge Performance	94.7%	92.3%	93.0%	93.7%
Power Management Interface Technology (% of Total Market)				
No Power Management Interface	34.5%	36.0%	36.5%	30.8%
Discrete Digital And Analog Signals Only	27.5%	21.3%	20.5%	20.0%
Serial Bus Interface Only	16.5%	20.8%	21.0%	25.0%
Mix Of Discrete Signals And Serial Comm. Bus	21.5%	22.0%	22.0%	24.3%
	100%	**100%**	**100%**	**100%**
Communication Protocol Type (% of Total Market)				
Customer Specific	1.3%	3.0%	2.3%	2.3%
Supplier Specific	11.3%	23.0%	22.5%	21.0%
Open Or Industry Std Bus (e.g. PMBus™)	76.0%	71.5%	72.8%	74.3%
Other Bus	11.3%	2.5%	2.5%	2.5%
	100%	100%	100%	100%

A new market is surfacing that was formerly hidden in the "other" market category: automotive and industrial power. With engine control, infotainment, and newer Advanced Driver Assist (ADAS) features; these areas have transient requirements similar to server applications, but with <10 A current requirements.

2) Trend Tables

TABLE VIII provides an example and readers are recommended to view the entire report for additional quantitative data.

VI. EMERGING TECHNOLOGIES

An important part of any Technology Roadmap is highlighting emerging technologies that could be significant to the industry. These technologies are not fully developed or in large volume production, but show promise as important game changers. This section features technology overviews written by industry experts in these fields. Two of the commentaries (3D packaging and additive manufacturing) focus on technologies that strive to increase power density to keep pace with increasing power demands of 3D digital circuits. Both include insight into the use of embedded components to shrink size, plus the ability to use additive manufacturing to print metal enclosures and heat sinks right in the laboratory. In addition, as densities increase, the need for smaller and more efficient thermal management devices continues to escalate. Liquid cooling is being implemented in a variety of mechanical configurations. The enclosed commentary highlights how the use of coolants with nanoparticles (nanofluid) can provide further improvements within a liquid-cooled system.

A. Trends in 3D Packaging of Power Products

Until recently, the packaging of power supplies was limited to what can be manufactured with machine and hand assembled multi-layer printed circuit boards with components on both sides. The emergence of embedded substrate technology was identified in the 2015 edition of the PTR [6] as having broad applicability to power supplies and converters. It provides the benefits of increased performance through lower parasitics, a smaller footprint, higher power density (W/cm^3), and lower cost ($/W/cm^3). Millions of units have been produced and shipped for everything from portable electronics to servers, automobiles, and industrial applications. However, in the majority of these products, only silicon semiconductor die are embedded. To continue to meet the needs of customers, it is essential the technology emerges that allows the cost-effective manufacture of embeddable Wide Band Gap (WBG) devices and power-capable capacitors and inductors.

The key market driver of this technology is to allow size and density improvements in the power converters as the loads of the power converter continue to shrink. While the size improvements will never scale with Moore's Law or the 'more than Moore' phenomenon, these techniques offer a path towards supporting the necessary power converter density improvements.

The biggest challenge is to find semiconductor, capacitor, inductor/transformer, and resistor companies to invest and market catalog products for 3D manufacturing; specifically, embedded substrates. Today, most will provide parts as custom designs for high-volume applications, and at a cost premium. The power industry can innovate faster with catalog available technology.

1) Semiconductors

There is now some maturity in the 3D packaging of semiconductor devices. Great progress has been made with both silicon and WBG devices manufactured for embedding or 3D assembly. The leading interconnect technologies are adhesives, solder, direct copper plating, and silver sintering. The embedded substrate designs are using a solder ball or other soldering technology for interconnection or are procuring die with copper terminations and directly plating to the die. The high-current products use either soldering to copper lead frames, plating to copper terminated die, or silver sintering. An emerging technology that is showing promise is Transient Liquid Phase Sintering (TLPS) [7], a liquid-assist sintering process during which a low melting point metal or alloy melts, surrounds, and diffuses into a different high-melting point metal. This system can be

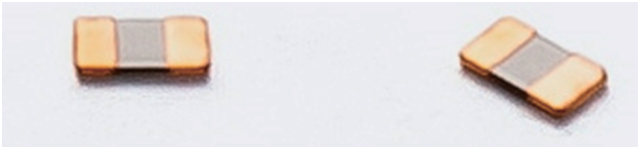

Fig. 7. Samsung embeddable capacitors 0.11 mm to 0.33 mm height.

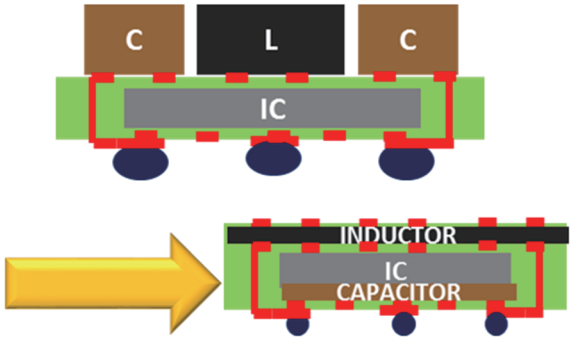

Fig. 8. Embedding of capacitor and inductor (Courtesy of Georgia Tech).

processed at low temperatures, but is capable of operating at the high melting point temperature of intermetallic compounds. Cu-Sn joints have been demonstrated that retain shear strength to T > 400 ºC. While many of the technologies are proven, the number of semiconductor or third-party companies willing to process die for 3D manufacture is still limited.

2) Capacitors

To further increase the density and decrease the size of 3D packaged power sources, it is essential that embeddable or stackable capacitors and inductors capable of higher currents and voltages become available. While several manufactures have been making custom capacitors in thin packages with copper termination, the first catalog parts designed for embedding just emerged in 2016. AVX has introduced its Ultra Thin (UT) series [8] with voltages up to 50 V at less than 0.35 mm thick. Samsung has introduced copper-terminated embeddable capacitors in case sizes from 0603 to 1005, with values up to 2.2 µF shown in Fig. 7.

For higher voltage applications, Kemet is giving presentations on DC-Link capacitors for WBG applications showing a COG MLCC 0.22 µF 500 V 150 ºC part [9]. The parts have a Ni/Thin Au termination and can be stacked using a CuSn TLPS process. ESR remains below 3 mΩ below 2 MHz. Single parts have been demonstrated up to 10 MHz. WBG devices allow for higher frequency operation that reduces the need for large capacitors, one possible path to higher density at higher voltages.

Strides are being made in nanoscale materials enabling embeddable tantalum capacitors. Georgia Tech's work on silicon-integrated nanoscale tantalum capacitors is moving toward the goal of passive integration of capacitors and inductors in standard dc-dc modules (Fig. 8) [10].

The core of the technology is a Tantalum foil, which enables the construction of a capacitor with the same electrical characteristics of a discrete Multi-Layer Ceramic Capacitor (MLCC) with only 40% of the thickness. High temperature and high

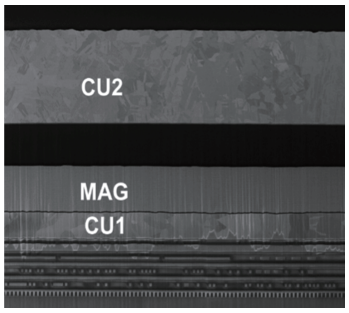

Fig. 9. SEM cross section of magnetic thin-film inductors integrated with CMOS IC.

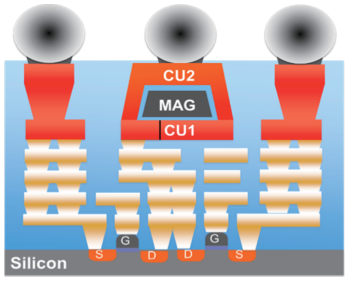

Fig. 10. Illustrated cross section of magnetic thin-film inductors integrated with CMOS IC.

voltage capacitors [10] with hybrid dielectrics composed of nanoscale inorganic and organic dielectrics are also in development targeting a density of 40 µF/cc at 450 V with operating temperatures up to 175 °C.

3) Magnetics

The introduction of high-permeability magnetic thin-films to CMOS manufacturing provides a new class of integrated inductor, enabling higher levels of integration and performance for applications that are currently relegated to using discrete inductors. Integrated magnetic thin-film inductors incorporate high permeability (µRel > 500), low coercivity (HC < 1 Oe), magnetic materials to provide a low reluctance path for the coil's magnetic flux, generating a significant inductance enhancement relative to air-core inductors [11]-[13]. These inductors can be fabricated with standard CMOS manufacturing processes and have a low profile (< 30 µm), which makes them compatible for monolithic integration with CMOS ICs as a back-end process option (Fig. 9, Fig. 10), or for embedding into a variety of packaging substrates on integrated passive devices (IPDs).

These inductors exhibit high inductance for a broad frequency band (> 1 GHz), high current density, and low dc resistance relative to existing on-chip inductor technologies. Integrated thin-film magnetic components will enable a new set of IC applications, such as integrated voltage regulation (IVR), where all components of a switched inductor dc-dc power converter are integrated on-chip. Integrated voltage regulation allows power to be delivered to ICs at higher voltages and then be efficiently down converted on-chip, reducing I^2R loss in the upstream power delivery network, and enabling improved power management with a larger number of independently scalable

on-chip power supplies [14]-[15].

The integration of dc-dc power conversion functions with CMOS provides substantial value in terms of volume, energy efficiency and cost for embedded, mobile and datacenter processors, power-management integrated circuits (PMICs), and other integrated circuit products. Until recently, applications of IVR have been hindered by the unavailability of appropriate integrated power inductors. The emergence of commercially available, thin-film magnetic core power inductors as a backend process option with a wide range of CMOS foundry offerings [16] is a major milestone that allows for application of IVRs to a wide range of computing platforms.

The primary challenges with adopting thin-film magnetic power devices for integrated voltage regulation include IC and system integration challenges in the applications that drive the need IVR. Existing power management architectures for microprocessors have been successively optimized over decades and tailored to individual applications. Commercial adoption of integrated magnetics in IVRs requires integration with these architectures, where board-level power converters shift towards the generation of a smaller number of power supplies with higher output voltage (1.8 V–3.3 V) and improved conversion efficiency to compensate for the introduction of an additional power conversion stage in the IVR. Likewise, microprocessor designers must learn to exploit the new capabilities of IVRs with integrated magnetics to realize all potential energy savings. The staggering complexity of modern computing systems compounds the challenge of introducing these architectural shifts and poses a significant challenge for rapid and large-scale adoption.

4) Manufacturing and Design

Until recently, the design and manufacture of 3D packaged power sources required a vast array of expertise. Printed circuit boards with embedded components can no longer be assembled in house or at a favorite contractor. A specialized vendor with expertise in imbedding, imbedded component procurement, and final testing is necessary. Expertise in sourcing semiconductor die with proper termination, flatness, and thickness is required. Which capacitor technology are you going use? Should you attempt to form your own in embedded substrate capacitors or buy embeddable capacitors? The same question applies to inductors and resistors. This has been a significant barrier to entry for many power source companies, but help is on the way. The first design and manufacturing partnership was announced in 2016 between UTAC and AT&S. UTAC is a leading assembly and test services provider and AT&S is one of the largest producers of embedded substrate power sources. Together, they can take a circuit, then design and manufacture an industry-leading 3D packaged power source using embedded substrate technology.

Many more companies are coming online as suppliers of embedded assemblies with some or all of the capability needed.

B. Additive Manufacturing

Additive Manufacturing (AM), now synonymous with 3D printing, has escalated in the last few years due to the expiration of several key patents held by companies like 3D Systems and Stratasys. In recent years, more clarity has been provided as many potential users defined succinct areas for needed development. Recently, the focus is broadening to Direct Digital Manufacturing [17] (DDM), of which 3D printing is a subset. Several topical areas are rapidly evolving: development of greater CAD visualization and definition tools with embedded multiphysics analytics that accelerate the design cycle; language definitions that capture material and object requirements to support integrated 3D additive, subtractive, and finishing manufacturing function; and, in particular, the move to multi-material processing that can provide spatial variation in heterogeneous material characteristics.

The challenge to developing AM for power electronic applications is finding proper materials that have been electrically characterized by the manufacturer, because the vast majority are for mechanical structures. The plethora of materials now being developed is not electrically characterized.

Work is progressing in applying 3D printing to WBG semiconductors and modules. The challenge is in the mechanical interface at the die metallization. Early work back in 1983 showed use of structured copper, which uses fine vertical cooper wires to make direct electrical and thermal contact to the die while providing stress relief. New printing approaches show the use of electron beam melting of Cu to Direct bonded copper (DBC) as a eutectic attach for Cu-metalized [18].

A substantial advantage would be printing metal on ceramic enabling power packaging which uses thin-printed metal with wire bonding capability [19].

To create integrated power modules that incorporate gate drives, etc.; direct writing of interconnects can be performed using metal loaded polymers (e.g. Ag-Epoxy). Again, this is not supporting thick metal interconnects as might be achieved in the direct writing on direct bond copper (DBC) or semiconductors as noted above. The power packaging laboratory, PREES, at North Carolina State University demonstrated a completed printed power module fashioned after the Vicor module, but with a gate drive integrated into the module lid, which used Ag loaded polymer [20].

More companies are creating machines for printing multilayer circuits. Using post process, electroplating for thicker outer conductors, such machines can quickly prototype gate driver circuits. The Nano Dimension [21], "DragonFly™ 2020 3D Printer deposits two materials, one conductive and one dielectric, in order to build a complete multilayer PCB from the bottom up. Each pass of the print head deposits dielectric and conductive material at the exact location specified by the design file. Starting from the underside conductive traces, the materials are built up to finish with the topside conductors. This process means that vias are built up, drop by drop, either as blind, open, or complete vias. Plated and non-plated through-holes are created by repeatedly leaving a space at a particular XY coordinate, thereby building surrounding materials up around a void. The dielectric ends up as a solid piece within which the conductive traces are positioned at the precise XYZ coordinates specified." This basic approach of Additive Multi-Material is not new science and could be scaled to full roll-to-roll manufacturing. This

shows great promise for AM at high volume.

The greatest impact to power electronics is the evolving developments in printed magnetics. Though powder-loaded polymers are readily available with fillers, such as graphite and ferrite; the introduction of nano-particles are assisting in densification for increasing desirable magnetic characteristics. Much of the work has been ongoing for military applications, but more industrially driven research is underway. Considerable efforts are now behind the development of fused deposition modelling (FDM)-based printed magnetics.

C. Nanofluids in Electronic Cooling

Power requirements for electronic devices have risen steadily in recent years, with the rate of increase sloping upwards, and that has necessitated enhanced thermal management solutions to preserve performance and maintain the mean time between failures (MTBF) of these devices. There are a variety of solutions that can be implemented for cooling high power electronic devices from air to liquid cooling. While air cooling is the default, liquid cooling is necessary when high-power electronic devices dissipate more than 300–520 W/cm^2 [22]-[23]. The addition of nanoparticles to a coolant (i.e. nanofluid) is an alternative that can provide further improvement within a liquid cooled system.

Engineered suspensions of nanoparticles in liquids have become known as nanofluids. The nanoparticles dispersed in a base fluid are typically metal or metal oxide particles with a size range of 1-100 nanometers. When suspended in the base fluid, nanoparticles create a colloidal solution that has been shown to eliminate the issues of erosion, sedimentation, and clogging that plagued earlier solid-liquid mixtures that used larger particles. Dispersion of nanoparticles in a base fluid alters the fluid's overall thermo-physical properties (such as enhancing the thermal conductivity). Researchers were able to demonstrate as much as 20% enhancement in heat transfer performance of a single-phase, liquid-cooled system when nanoparticles were introduced [24].

The idea of using liquid cooling for power electronics applications is no longer confined to theoretical observations or laboratory experiments. There is widespread use of heat pipes, for example, and personal computers frequently incorporate elaborate liquid cooling systems. Nanofluids represent an enhancement to the technologies that are increasingly being used for cooling electronics.

Much of the ongoing research is focused on immersion cooling and boiling. In tests, boiling with nanofluids has been shown to improve the value of critical heat flux (CHF) by as much as 200% as a result of nanoparticle deposition on the surface of component. This has led to other research on engineering the surface of high-powered electronic devices with nanoparticles to improve heat dissipation without the need for an engineered liquid.

Researchers are also continually testing new materials to disperse in different fluids: aluminum oxide, iron oxide, zinc oxide, cerium oxide, and bismuth oxide are just some of the options that Nanophase Technologies Corporation offers to customers. In addition, there is work being done with carbon nanotubes that have shown promising results in heat transfer [25]. New materials, such as graphene, are also being developed and tested to determine their potential for application in thermal management.

Other trends in the technology include the use of different materials: Copper, aluminum, and newly developed polymers for the loop of a liquid cooling system or different wicking materials in the production of heat pipes and vapor chambers. In addition, improvements are being made in heat exchangers, pumps, and other components of liquid cooling systems.

While nanofluids have gained momentum in the past two decades, there are still several challenges to their widespread commercialization [26]. One of those challenges is that the concept of nanofluids is still relatively young. The term was only coined in the early 1990s and, while the number of studies has increased in recent years, there are no long-term assessments of how the addition of nanoparticles could affect a cooling system over time. Nanoparticles could collect and cause degradation in a pump or heat exchanger, for example. There is a widespread belief in the stability and reliability of nanofluid solutions, but it has not been possible to document that over a long period of time.

Questions have been raised about the environmental impacts of disposing of nanofluids from a system, whether as vapor, in the case of a nuclear power reactor, or as liquid, when replacing the fluid in a data center system. While it is possible that nanoparticles in high quantities could be harmful, there are few studies that have focused on the environmental impacts [27] or the impact on humans [28].

VII. Conclusion

The discussion herein is just a snapshot in time. PSMA has been publishing these roadmap reports for almost twenty five years, and development activity relating to the next edition is already underway. Technologists who are interested in participating or contributing are encouraged to contact the authors or the PSMA office.

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Analysis and Design of a 1200 V *All-SiC* Planar Interconnection Power Module for Next Generation More Electrical Aircraft Power Electronic Building Blocks

Mattia Guacci, Dominik Bortis, Ivana F. Kovačević-Badstübner, Ulrike Grossner, and Johann W. Kolar

***Abstract*—Compact, light weight and efficient Power Electronic Building Blocks are seen as fundamental components of future *More Electric Power Systems*, e.g. *More Electrical Aircraft*. Core elements supporting the trend are power modules employing solely SiC MOSFETs. In order to take advantage of the high switching speed enabled by SiC, novel modules concepts must be investigated. For example, low inductance planar interconnection technologies, integrated buffer capacitors and damping networks are possible solutions to mitigate switching overvoltages and oscillations at the switching node occurring for conventional modules. In this paper, the analysis and the design of a novel ultra-low inductance 1200 V SiC power module featuring an integrated buffer-damping network are discussed. The power module is first described and characterized with impedance measurements. Afterwards, a general optimization procedure for the sizing and the selection of the integrated components is presented and measurements are performed to verify the analysis and to highlight the improvements of the proposed solution.**

***Index Terms*—*All-SiC* Power Module, Damping Network, Integrated Buffer Capacitor, Planar Interconnection Technology.**

I. Introduction

THE *More Electrical Aircraft* (MEA) concept targets the replacement of mechanic, pneumatic and hydraulic systems of commercial aircraft with electric power converters and actuators, aiming for decreased fuel consumption and/or emissions reduction, increased reliability and/or lower maintenance effort [1]. The turning point of the trend can be traced back to 2010, when the milestone of 1 MVA of electric power was reached on board of *Boeing*™ B787. An electric power requirement of 1.6 MVA is planned for the next generation of aircraft [2], motivating the increased interest of the power electronics community in MEA. In particular, the *Horizon*2020 European. Project 636170 - Integrated, Intelligent Modular Power Electronic Converter (I2MPECT) [3], building on the expertise in device packaging, thermal management, converter design and reliability analysis of European industry and academia, intends to demonstrate significant advances in terms of powerto-weight ratio and efficiency of power converters for MEA. The primary goal is the realization of a *Power Electronic Building Block* (PEBB), i.e. a 99% efficient 3-phase inverter (cf. TABLE I) achieving a power-to-weight ratio of 10 $\frac{\text{kW}}{\text{kg}}$, i.e. three times higher than nowadays available solutions [4].

TABLE I
Electrical Specifications of the I2MPECT Power Electronic Building Block

	Description	Value
V_{dc}	input DC voltage	540 V, ... 700 V
f_{sw}	switching frequency	30 kHz
v_{out}	output AC voltage	110 V_{RMS}
$i_{out,\,ph}$	output AC current per phase	190 A_{pk}
$P_{out,\,ph}$	output power per phase	15 kVA
f_{out}	output frequency	400 Hz, ... 2 kHz

PEBBs, i.e. modular power converters with defined functionality and simplified interfaces, combined with switching stages based on power modules employing solely Silicon Carbide (SiC) semiconductors (*All-SiC* PMs), can push the already strict requirements concerning compactness and light weight established in the aircraft industry even further, while still enabling reduced complexity and costs. The PEBBs approach reduces the engineering effort both in the design and in the maintenance phase of a power electronic system while SiC intrinsic qualities, e.g. higher switching speed, lower on-state voltage and improved temperature withstanding capability allow a reduction of the losses, output filter downsizing and low cooling requirements [5]. However, in order to guarantee the reliability of the PEBB and to fully utilize SiC performance, an ultra-low inductance PM designs is required. In fact, parasitic inductances in combination with the enabled high switching speed could cause significant overvoltages and undesired ringing [6]. This ultimately compromises the lifetime of the PM and increases its electromagnetic noise emissions [7].

To explore the state-of-the-art in terms of commutation

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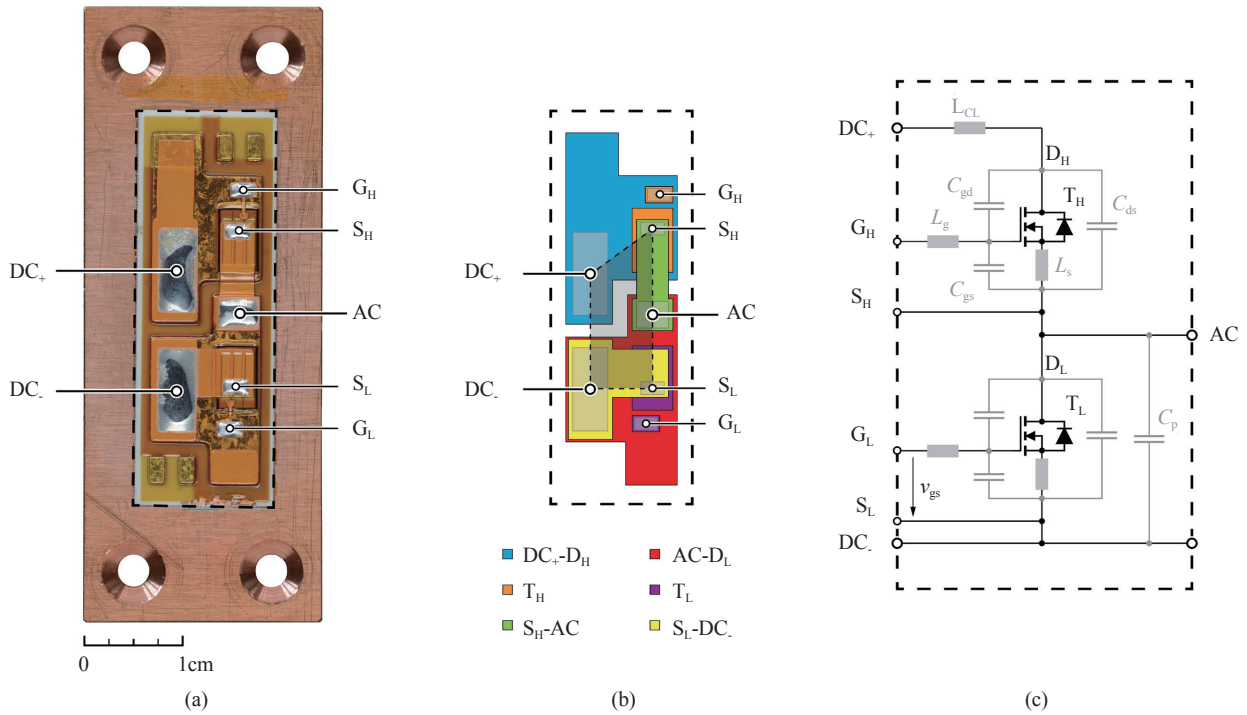

Fig. 1. Prototype of the designed PM including two 1200 V SiC power MOSFETs (*Cree*™ CPM2-1200-0025). The solder pads for gate (G_L, G_H) and Kelvin source (S_L, S_H) connections are highlighted, as well as the DC and AC terminals of the half-bridge (a). The structure of the PM is clarified with colors (b): the planar interconnections (green and yellow) and the substrate copper layer (blue and red) enable an ultra-low inductance design. The area of the average commutation loop is highlighted. Finally, the equivalent circuit of the PM, including parasitic capacitances and inductances, is illustrated in a schematic (c).

loop inductance L_{CL} in 1200 V *All-SiC* PMs [8]–[10], a comprehensive analysis of commercially available PMs is conducted. Most of nowadays available designs employ bond wires to interconnect the dies and feature L_{CL} values in the range of 10 nH to 30 nH (cf. TABLE II). In order to allow a fair comparison between the PMs, a figure-of-merit is defined as

$$\mathrm{FOM} = \left(\frac{R_{\mathrm{ds}} I_{\mathrm{ds}}^2}{V_{\mathrm{dc}} I_{\mathrm{ds}}} \; 100 \; \frac{L_{\mathrm{CL}}}{1\,\mathrm{nH}} \right)^{-1} . \qquad (1)$$

The lower limit of L_{CL} only slightly reduces to around 6 nH if research prototypes are considered [11]–[15]. Differently, when planar interconnection technologies are considered [16], [17], i.e. bond wires are replaced by wide coplanar structures [18], L_{CL} can be reduced below 2 nH [19], [20] (cf. TABLE III). PMs adopting this solution provide benchmarks for the next generation of PMs. Additionally, planar interconnection technologies facilitate symmetric designs and enable doublesided cooling [7], [21] aiming towards an even increased power density.

A second measure allowing the utilization of SiC high switching speed is the integration of a buffer capacitor in the PM. It allows the decoupling of L_{CL} from the parasitic inductance (L_{ext}) of the connection between the PM and the external input filter capacitor [11]. If a sufficient amount of capacitance is selected, the current during the switching transient is provided from the integrated capacitor and only the portion of inductance inside the PM (L_{CL}) experiences a fast current variation di/dt [22], mitigating the overvoltage. On the other hand, the paralleling of the buffer capacitor with the external capacitor introduces an undamped resonance network. Therefore, in order to prevent prolonged oscillations, a suitable damping network must be additionally integrated.

Ultimately, the sizing of the buffer capacitor and of the optimized damping network result from a trade-off between required volume and effectiveness of the solution. Moreover, the impact of parasitic inductances, e.g. L_{CL} and L_{ext}, on the performance of the buffer-damping network is not known in advance and therefore a widely applicable approach is desired. Accordingly, the focus of this paper is first on the design and experimental analysis of an *All-SiC* PM half-bridge arrangement featuring planar interconnections; second, the design procedure for an optimized integrated buffer-damping network with low sensitivity towards parasitic inductance is discussed. In order to experimentally validate the benefits enabled from a low inductance PM design and explore its limit, the PM prototype of Fig. 1 (a), featuring a planar interconnection technology, is characterized in Section II. The effectiveness of an integrated buffer capacitor against overvoltage is proven with measurements in Section III. Subsequently, in Section IV, the optimization of an integrated damping network is discussed and its performance are analyzed. Afterwards, a guideline for a general design procedure is described in Section V. Finally, conclusions are

TABLE II
COMMUTATION LOOP INDUCTANCE OF COMMERCIALLY AVAILABLE 1200 V *ALL-SIC* PMS

Manufacturer	I_{ds} (A)	$R_{ds,on}$ (mΩ)	L_{CL} (nH)	FOM
Cree™	138	13.0	15	0.45
	285	5.0	14	0.60
	256	3.6	5	2.60
Rohm™	180	7.8	25	0.34
	300	4.7	13	0.65
Semikron™	523	5.6	15	0.27

TABLE III
COMMUTATION LOOP INDUCTANCE OF *ALL-SIC* PMS IMPLEMENTING PLANAR INTERCONNECTIONS

Research Facility	V_{dc} (V)	I_{ds} (A)	L_{CL} (nH)
Univ. of Notthingham, et al. [23]	2500	-	1.7, ... 2.6
Univ. of Grenoble, et al. [7]	1200	144	< 2
Univ. of Tennessee, et al. [24]	1200	-	2.6
Fraunhofer™ IZM, et al. [19]	-	-	0.9
Semikron™ [20]	1200	400	1.4

drawn in Section VI.

II. ULTRA-LOW INDUCTANCE *ALL-SIC* PM

The one to one replacement of Si MOSFETs and IGBTs in PMs with SiC MOSFETs does not allow the full exploitation of SiC performance: the enabled high switching speed, in fact, sets more severe constraints on the values of parasitic elements that can be tolerated. Therefore, new challenges during the design phase of *All-SiC* PMs must necessarily be faced.

In this section, the PM prototype shown in Fig. 1 is characterized, stressing the importance of dies positioning and interconnection technology in order to achieve an ultra-low inductance design. Considerations are deliberately limited to a basic but modular half-bridge structure (i.e. only one die per switch), designed for the specifications reported in TABLE I but for one sixth of the power rating.

A. Analysis of the PM Prototype

The PM shown in Fig. 1 consists of two *Cree*™ CPM2-1200-0025 SiC power MOSFETs (4 mm×6.4 mm) connected in bridge-leg configuration by a patented planar interconnection technology [16]. In Fig. 1 (b), the arrangement of dies and the terminals are highlighted. The high-side MOSFET T_H (orange) is pressure silver sintered on the upper (blue) substrate copper layer (300 µm thick) connecting its drain D_H (on the back-side of the die) to the positive supply terminal DC_+. Similarly, the low-side MOSFET T_L (purple) is sintered on the bottom (red) substrate copper layer connecting its drain D_L to the AC output. The source contacts of the MOSFETs (S_H and S_L on the top-side of the dies) are connected depositing a copper layer forming the planar interconnections (100 µm thick) from S_H to AC (green) and from S_L to DC_ (yellow). A 50 µm thick polyamide-base material isolates the substrates from the interconnections.

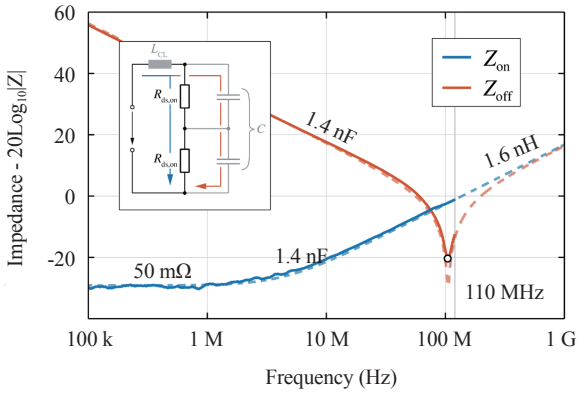

Fig. 2. Impedance measured from the DC terminals of the PM shown in Fig. 1 when (blue) both MOSFETs are conducting and (red) blocking. Series *RL* and *LC* equivalent circuits (dashed) with the values given in the figure match the measurements respectively. For frequency higher than 110 MHz, only the simulated curves converging to L_{CL} = 1.6 nH are shown.

Because of the selected technology, only one copper layer is available, therefore is not possible to overlap yellow and green connections aiming to a vertical design which would yield to an even lower L_{CL} [18]. The area of the horizontal commutation loop (highlighted in grey), including the DC terminals and the MOSFETs, is minimized, whereas the distances are only constrained by the manufacturing process and/or isolation requirements. The overall size of the Al_2O_3 ceramic substrate (dashed in Fig. 1 (a)-(c)) results 39.4 mm×13.8 mm with an overall maximum thickness of 1.3 mm.

B. Commutation Loop Inductance

In order to verify the effectiveness of this design solution, L_{CL} is characterized with multiple impedance measurements. The measurements are conducted with a precision impedance analyzer *Agilent*™ 4294A in combination with the adapters 42941*A* and 16047*E*. Different adapters and connections to the PM influence the measurement, however the relative standard deviation results below 10%.

More in detail, when both MOSFETs are conducting, the circuit seen from the DC terminals of the PM can be approximated by a *RL* series connection, where $R = 2R_{ds,on}$ and $L = L_{CL}$. Differently, when both MOSFETs are in the blocking state, the impedance resemble a *LC* series connection, where $L = L_{CL}$ and

$$C = \frac{1}{2}\left(\frac{C_{gs}C_{gd}}{C_{gs}+C_{gd}} + C_{ds}\right) = \frac{1}{2}\left(C_{oss} - \frac{C_{rss}^2}{C_{iss}}\right) \quad (2)$$

is defined by the parasitic capacitances of the two SiC MOSFETs connected in series (neglecting C_P). The impedance of ideal *RL* and *LC* equivalent circuits are analytically calculated in the frequency domain and the value of *R*, *L* and *C* are selected in order to best approximate the measured curves, as

shown in Fig. 2. The value of $R_{ds,on}$ is additionally measured during the conduction of a DC current where, in accordance with [25], approximately 25 mΩ results for each MOSFET; moreover, inserting in (2) the values of the parasitic capacitances specified in [25] for v_{ds} = 0 V, an equivalent capacitance C = 1.4 nF results as expected. Even if the frequency measurement range of the instrument is limited to 110 MHz, the analytical curves clearly converge to the extrapolated value of L_{CL} = 1.6 nH.

Remark: nowadays, the evaluation of L_{CL} is typically entrusted to the electromagnetic modelling of the PM supported by specialized softwares, such as *Ansoft*™ *Q3D* [12]–[14]. According to the trend, the 3D CAD file provided from the PM manufacturer is imported in *Q3D* and, after simulating the described experiment, L_{CL} = 2.7 nH results. The relative discrepancy is significant and the simulated value shows excessive variations depending on the setting of the excitation ports in the simulation tool. This issue is under investigation [26], however the cause is identified in the hypothesis of equipotential excitation ports, ultimately representing the boundary conditions for the simulated electromagnetic problem.

C. Gate Loop Inductance

The connection from the PM to the gate driver plays an important role in the shaping of the voltage and current waveforms during a switching transient. In a first approximation, the path from the driver to the gate connection on the die can be represented with the inductance L_g shown in Fig. 1 (c). Intuitively, L_g limits the changes of the gate current, reducing the bandwidth of the driver. This consequently increases the delay time and the current rise time, ultimately increasing the switching losses [27].

Additionally, the charging process of C_{gs} excites a resonance at $f_g = 1/2\pi\sqrt{L_g C_{gs}}$ and, in order to limit v_{gs} below the gate voltage rating of the MOSFET, a lower boundary for the gate resistance $R_{g,lim}$ is set. $R_{g,lim}$ is proportional to L_g, but while being effective in damping the resonance, it also limits the maximum switching speed.

Based on the premises above, it is clear that the minimization of the gate connections length should be of main concern for the design of a PM. The integration of the gate driver is only ideally a valid option, because it requires additional effort, leads to higher costs and size, and increases the failure rate of the PM [28]. Short, wide and coplanar connections are more realistically advised as best practice. For convenience, however, gate and source terminals are typically routed all together and next to each other to one side of the PM. Adopting this approach, the value of L_g can easily reach 30 nH [11], resulting in the mentioned drawbacks.

Additionally, if the connection to the source of a MOSFET is partially shared between gate driver and bridge-leg, a fraction of L_g (L_s in Fig. 1 (c)), known as common source inductance, is shared with the path defining L_{CL}. Consequently, a change on i_{ds} directly affects v_{gs} according to

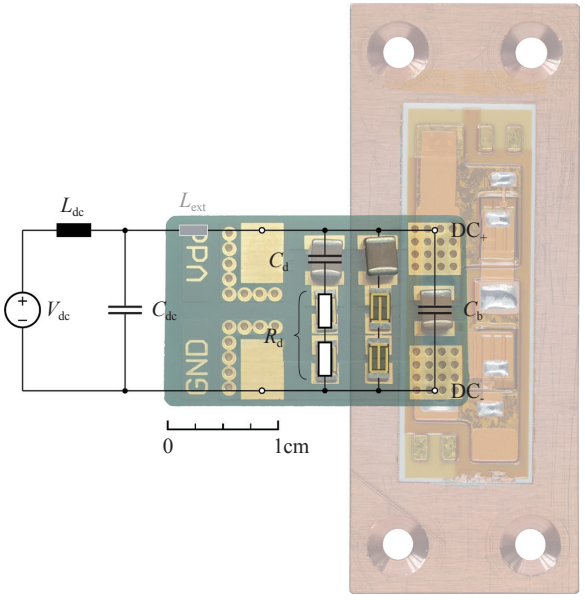

Fig. 3. 1 mm-thick PCB providing a practical and low inductive solution to integrate the buffer capacitor C_b and the damping network R_dC_d in the PM. One undamped and two damped 1210 *Kemet*™ 1500 V *X7R* ceramic capacitors find place together with power resistors of different values.

$$v_{gs} = v_{gs,0} - L_s \frac{di_{ds}}{dt}. \tag{3}$$

E.g. with a current slope of 10 $\frac{A}{ns}$, each 100 pH of L_s subtracts 1 V from $v_{gs,0}$ during a turn-on transition, providing a negative feedback reducing the switching speed. This issue is well known and can be avoided splitting the power source and the gate source connection, i.e. Kelvin source. It is less transparent, instead, that even if L_g and L_{CL} are physically independent, the magnetic coupling between them ($M_{g,CL}$) basically plays the same role as L_s. Although it is difficult to experimentally quantify the impact of $M_{g,CL}$ on v_{gs}, it is important to be aware of its consequences once the gate driver is arranged in the close proximity of the PM.

In the considered PM, gate and Kelvin source solder pads are directly accessible from the top of the dies (G_L, G_H and S_L, S_H indicated in Fig. 1 (a)). In particular, S_H directly contacts T_H and is separated from the copper interconnection carrying the load current to AC (yellow); the same applies for S_L, separated from DC_. Short and wide copper connections are used to connect the solder pads to the driver, reducing L_g to only 6 nH. In this way, low values of R_g could be selected, achieving high switching speed therefore minimizing the switching losses without the risk of damaging the gate dielectric. With the aim of further reducing L_g, a solution featuring overlapping gate connections on a flexible PCB could be used. In the case at hand, *Q3D* simulations performed on the complete setup [26], obtained by merging the CAD file of the PM and of the gate driver PCB, showed negligible coupling.

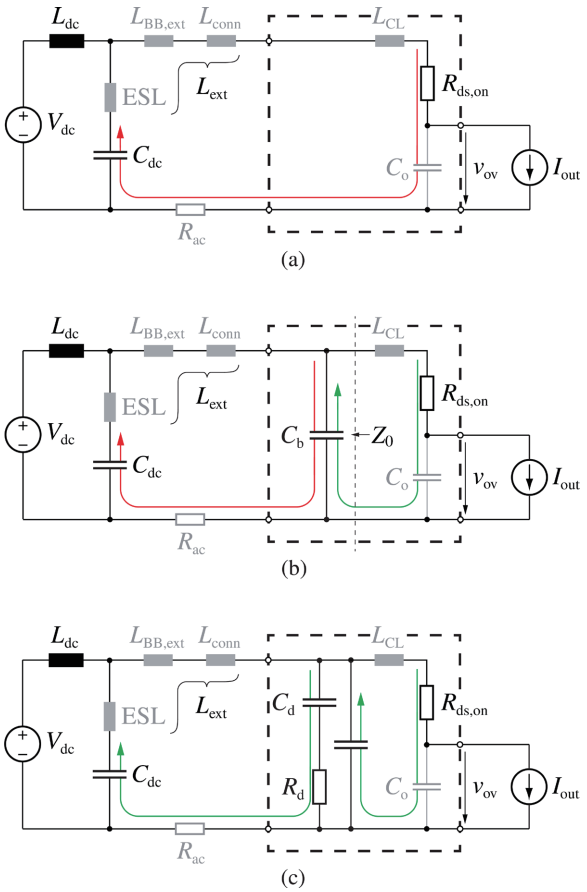

Fig. 4. Equivalent circuit of the analyzed half-bridge in a DPT setup during a hard turn-on switching transition. In (a), the high-frequency current components excited from the switching transition flow through L_{ext}, leading to overvoltage across the low-side MOSFET T_L (i.e. v_{ov}) after turn-off. With the integration of C_b (b) in the PM (dashed box), the high-frequency currents are confined (green), but a resonance network between L_{ext} and C_b is created, causing severe ringing at v_{ov}. In (c), a damping network R_dC_d is additionally integrated to damp the ringing. The output impedance Z_0 of the input filter is measured as indicated.

III. Integrated Capacitive Snubber

The amount of capacitance necessary at the DC side of a converter (C_{dc}) can vary in a wide range depending on the power rating and input voltage V_{dc} and it typically results in a bulky structure (e.g. $C_{dc} \approx 100$ µF in the considered setup) that hardly finds place in the closest proximity of the switching stage, i.e. the PM. The inductances of the conductors connecting C_{dc} to the DC terminals of the PM significantly contribute to the total power loop inductance $L_{PL} = L_{ext} + L_{CL}$. In particular, its ideal lower boundary is limited by the parasitic inductance of C_{dc} (ESL), typically in the order of 10 nH to 20 nH [29]. A significant L_{ext} vanishes the benefit of a low inductance PM design, therefore a possible solution, i.e. the integration of a buffer capacitor in the PM (cf. Fig. 3), is analyzed in this section.

The circuit supporting the first part of the explanation is shown in Fig. 4 (a). It represents the PM of Fig. 1 (dashed box) connected in a Double Pulse Test (DPT) setup and simplified for the case of a hard turn-on switching transition of the high-side MOSFET T_H. The parameters of the DPT setup and the values of the parasitic elements introduced in Fig. 4 (a) are summarized in TABLE IV (herein $L_{ext} = 15$ nH and $R_g = 1.5\ \Omega$ if not differently specified).

TABLE IV
Parameters of the DPT Setup and Parasitic Elements of the PM

	Description	Nominal Value
T_H, T_L	*Cree*™ CPM2-1200-0025	1200 V, 90 A
I_{out}	switched output current	30 A
V_{dc}	input DC voltage	540 V
C_{dc}	external film capacitor	94 µF, 800 V
L_{dc}	input inductor	1 mH
R_g	gate resistance	1.5 Ω or 5 Ω
L_g	parasitic gate inductance	6 nH
v_{gH}	T_1 gate driver voltage	$V_{on} = 20$ V
v_{gL}	T_2 gate driver voltage	$V_{off} = -5$ V
C_b	buffer capacitor	0, ... 24 nF
C_d	damping capacitor	0, ... 24 nF
R_d	damping resistor	0.5 Ω, ... 4.7 Ω
$R_{ds,on}$	high-side MOSFET on-state resistance	25 mΩ
R_{ac}	frequency dependent resistance	0.2 Ω, ... 0.7 Ω
C_o	switching node parasitic capacitance	260 pF
L_{CL}	commutation loop in the PM	1.6 nH
L_{conn}	PM connectors	6 nH
$L_{BB,ext}$	from PM connectors to C_{dc}	0 nH or 20 nH
ESL	C_{dc} parasitic inductance	9 nH
L_{ext}	$L_{conn} + L_{BB,ext} + ESL$	15 nH or 35 nH

A current step through *Lext*, originating from the switching transition, excites the resonance between L_{PL} and C_o ($C_{dc} \to \infty$). C_o represents the parallel connection of the output capacitance (C_{oss}) of the low-side MOSFET T_L with the parasitic capacitance of the PM from the switching node to DC_ (C_p cf. Fig. 1 (c)). While the latter depends only on the geometry of the PM (i.e. $C_p = 45$ pF), C_{oss} is non-linear, i.e. $C_{oss}(v_{ds})$; however, in order to best model the resonance occurring on a DC voltage bias, $C_{oss}(V_{dc}) = 215$ pF [25] is considered. This results in $C_o = 260$ pF.

The frequency dependent parasitic resistance $R_{ac}(f) > R_{ds,on}$ of the $L_{PL}C_o$ resonant network, typically much smaller than its characteristic impedance, $\sqrt{L_{PL}/C_o} \approx 8\ \Omega$, is the only damping element present. Consequently, a voltage spike and a prolonged oscillation at the voltage v_{ov} across T_L occurs, as shown in blue in Fig. 5. v_{ov} reaches 896 V ($v_{ov,pk}$), more than 300 V above V_{dc}, and strongly oscillates when $R_g = 1.5\ \Omega$. This waveform provides other information on the parameters of the equivalent circuit of Fig. 4 (a). Knowing C_o, L_{PL} can be calculated from the resonant frequency $f_{tot} = 1/2\pi\ 1/2\pi\sqrt{(L_{CL}+L_{ext})C_o} = 77$ MHz and 16.6 nH results as expected ($L_{PL} = L_{ext} + L_{CL} = 15$ nH + 1.6 nH). Additionally, analyzing the exponential decay of

$$v_{ov}(t) = V_{dc} + (v_{ov,pk} - V_{dc})e^{-t/\tau}, \tag{4}$$

with a time constant of $\tau = 48$ ns, $R_{ac}(f_{tot}) = 0.7\ \Omega$ results. The

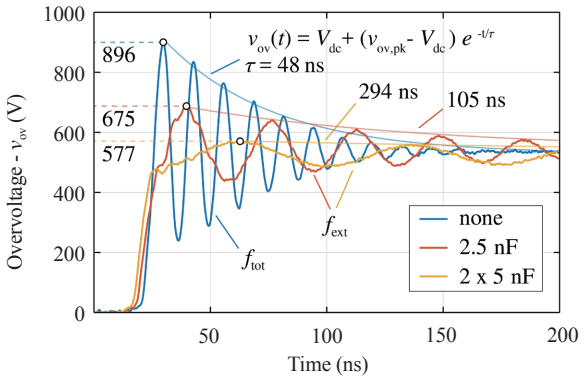

Fig. 5. Measured waveforms of the voltage across T_L during hard turn-on switching transition of T_H (i.e. R_g = 1.5 Ω, L_{ext} = 15 nH) with (red and yellow) and without (blue) integrated buffer capacitor C_b. A C_b bigger than 2.5 nF already significantly reduces the peak of v_{ov}, however, without a proper damping network, a prolonged oscillation occurs.

value of R_{ac} completes the linear model shown in Fig. 4 (a), enabling the simulation of the waveforms of v_{ov}; hence, the oscillation after the switching transient and its decay can be compared with measurements. However, correct initial conditions, i.e. the amplitude of the current step $i_{out,pk}$ exciting the resonance, must be set and therefore must be known in advance. For this reason, a measurements-based approach is initially preferred to optimize the buffer-damping network.

With the integration of the buffer capacitor C_b in the PM, as shown in Fig. 4 (b) and Fig. 3, L_{PL} is split in L_{ext} and L_{CL}, and L_{CL} is minimized. Consequently, the high frequency current components excited during the switching transient are confined in a smaller loop (green in Fig. 4 (b)) and bypass L_{ext}, significantly reducing $v_{ov,pk}$. With the final goal of quantifying the achievable improvements and dimensioning C_b, several experiments are performed.

Two measured waveforms (red and yellow) are shown in Fig. 5 for two different values of C_b = 2.5 nF and 10 nF. The main resonant frequency is now shifted to $f_{ext}=1/2\pi\sqrt{L_{ext}C_b}<f_{tot}$ (f_{ext} = 26 MHz and 13 MHz, respectively) because $C_b > C_o$ and $L_{ext} \approx L_{PL}$. Due to the lower resonant frequency, R_{ac} reduces ($R_{ac}(f_{ext}) \approx 0.1$ Ω,...0.2 Ω) and correspondingly increases to 105 ns and 294 ns, prolonging the oscillation.

Moreover, connecting C_b, a second resonant network resonating at $f_{int} = 1/2\pi\sqrt{L_{CL}C_{oss}}$ = 247 MHz > f_{tot} (because L_{CL} < L_{PL}) is formed. The associated oscillation is only partially visible on the waveforms, given the ultra-low inductance design and the higher value of frequency dependent resistance. Nevertheless, if needed, it can be damped at the AC side of the PM [30]. However, it is worth noticing that, if f_{int} exceeds the parasitic frequency of the output filter, less attenuation might be guaranteed from it.

Fig. 5 provides an additional information on the effective capacitance of C_b. In this setup, C_b is implemented by connecting one or more *Kemet*™ 1500 V *X7R* ceramic capacitors [31] with values between 4.7 nF and 12 nF in parallel (cf. Fig. 3). A reduction of capacitance, due to the DC voltage offset, is expected and confirmed from the measurements.

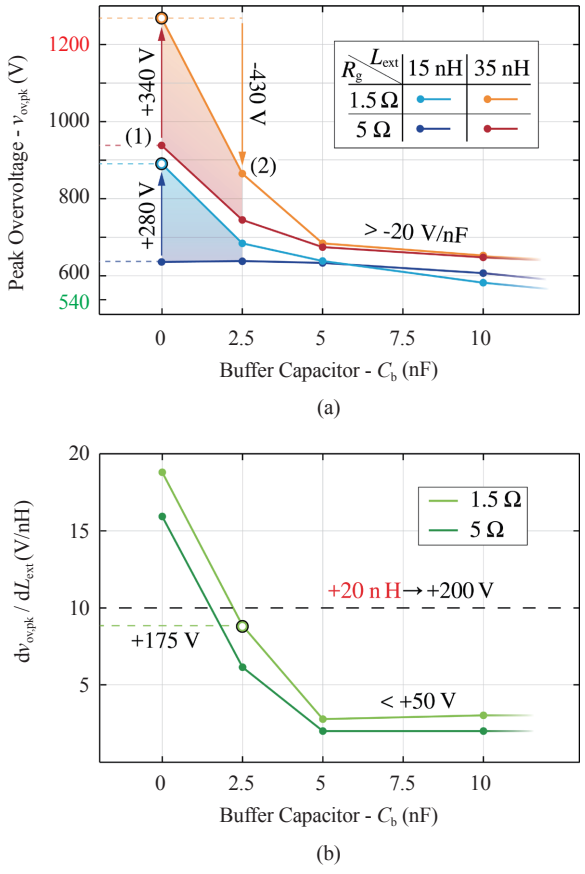

Fig. 6. Measured peak of v_{ov} during hard turn-on switching transition of T_H with respect to C_b for four different combinations of L_{ext} and R_g (a). Without C_b, L_{ext} = 35 nH and R_g = 1.5 Ω cause v_{ov} to exceed the voltage rating of CPM2-1200-0025 (i.e. 1200 V). Additionally, the sensitivity of $v_{ov,pk}$ towards L_{ext} is plotted (b). Without C_b it is above 15 $\frac{V}{nH}$, while with C_b bigger then 5 nF, it is limited below 3 $\frac{V}{nH}$ in both cases.

Knowing L_{ext} and measuring f_{ext}, the effective value of C_b can be calculated in the different cases; the resulting capacitance is always approximately half of the nominal value $C_{b,nom}$. For the sake of clarity, the reported value of capacitance always refers to the effective one.

Overvoltage and oscillation can become more severe in case of higher switching speed or in designs featuring bigger L_{ext}. Fig. 6 (a) summarizes $v_{ov,pk}$ for different combinations of R_g and L_{ext} which, without C_b, have a strong influence on $v_{ov,pk}$. As can be noted, L_{ext} = 35 nH and R_g = 1.5 Ω cause v_{ov} to exit the Safe Operating Area (SOA) of the MOSFET. Increasing R_g to 5 Ω (1-red) or integrating C_b = 2.5 nF (2-orange) is almost equally effective against $v_{ov,pk}$. However, the second option guarantees a better trade-off with respect to switching losses [32]. Clearly, the setup featuring smaller L_{ext} (light and dark blue) shows reduced $v_{ov,pk}$ in the same conditions.

C_b = 2.5 nF is sufficient to maintain $v_{ov,pk}$ < 900 V for all the considered combinations. Increasing C_b to 5 nF is only effective on the worst case (orange), whereas C_b > 5 nF brings no real further improvement from this point of view. This is clarified in Fig. 6 (b), where the sensitivity of $v_{ov,pk}$ towards L_{ext} is plotted. Almost independently from R_g, the sen-

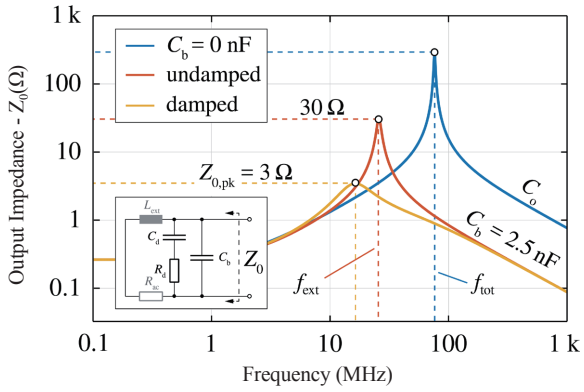

Fig. 7. Output impedance of the C_b-R_dC_d network (Z_0) for C_b = 2.5 nF with (yellow) and without (red) the damping network. The optimized damping network (R_d = 1.5 Ω and C_d = 5 nF) reduces $Z_{0,pk}$ from 30 Ω to 3 Ω according to the specifications. The impedance without C_b seen from the AC terminal is also plotted (blue) to highlight the shifting of the main resonance from f_{tot} to f_{ext}.

sitivity $\mathrm{d}v_{ov,pk}/\mathrm{d}L_{ext}$ drops from 15 $\frac{V}{nH}$ (without C_b) to 3 $\frac{V}{nH}$ (C_b > 5 nF). For the rest of the analysis the value of C_b is fixed to 2.5 nF ($C_{b,nom}$ = 4.7 nF).

To conclude, it is worth mentioning once again that the performance of this solution (i.e. integration of C_b) are supported by the ultra-low inductance PM design (i.e L_{CL} = 1.6 nH). For example, assuming L_{CL} = 15 nH, it is clear that no value of C_b could reduce $v_{ov,pk}$ below the limit obtained with L_{ext} = 15 nH and without C_b integrated in the PM (i.e. 896 V).

IV. Damping Network Optimization

As discussed in Section III, C_b effectively limits $v_{ov,pk}$ and relaxes the design constraints on L_{PL}, but indirectly modifies the impedance of the input filter (Z_0 in Fig. 4 (b)) as shown in Fig. 7. As a consequence, the main resonant frequency, clearly visible at the output voltage v_{ov}, is shifted from f_{tot} to $f_{ext} < f_{tot}$. As described in Section III, due to the reduction of R_{ac}, less damping is provided and the oscillation is prolonged. Then, with the considered values, fext enters the regulated EMC spectrum (f_{ext} < 30 MHz) negatively affecting the electromagnetic noise compatibility of the PEBB. Finally, the ringing at v_{ov} reflects on the current flowing through C_{dc}; the comparable amplitude and reduced damping degrade its lifetime.

This premise motivates the analysis and the optimization of a damping network presented in this section. Different damping solutions are discussed in literature [33]; the simplest damping approach avoiding steady-state losses is a series R_dC_d network in parallel with C_b [34], [35] (cf. Fig. 3 and Fig. 4 (c)). This approach is selected to facilitate the integration in the PM. In first place, a design procedure should be defined to dimension R_d and C_d, once L_{ext} and C_b are fixed. [33] proposes an optimization routine that, given the maximum allowed peak of the buffer-damping (C_b - R_dC_d) network output impedance ($Z_{0,pk}$), provides the value for R_d and C_d ensuring optimal damping, i.e. minimizing C_d.

TABLE V
Components Value for the Optimized Snubbers with $Z_{0,PK}$=3 Ω

L_{ext} (nH)	C_b	$C_{b,nom}$ (nF)	C_d	$C_{d,nom}$ (nF)	R_d (Ω)
15	2.5	4.7	5.0	12	1.5
35	2.5	4.7	10	24	2.0

This closed form procedure is preferred over an analytical approach [36]. In order to explore the effectiveness of this solution, a wide set of measurements with damping network featuring different combinations of R_d and C_d is performed and the results are commented in the following.

Fig. 8 (a) shows $Z_{0,pk}$ for different R_d-C_d pairs in the range 0.5 Ω < R_d < 10 Ω and 2 nF < C_d < 10 nF with L_{ext} = 15 nH, C_b = 2.5 nF and R_{ac} = 200 mΩ. Onlythree values for R_d (0.5 Ω, 1.5 Ω and 4.7 Ω) and C_d (2.5 nF, 5 nF and 10 nF) are considered in the experiments. Thus, the highlighted nine different combinations for R_d and C_d, having $Z_{0,pk}$ in the range between 1.8 Ω and 9.4 Ω, are analyzed. The performance of the damping network outside this range rapidly decay. In Fig. 8 (b)-(d), the corresponding measured waveforms of v_{ov} are illustrated.

Because of the additional capacitance C_d and resistance R_d, $v_{ov,pk}$ is now limited to values below 600 V, even if C_b = 2.5 nF is considered. As shown in red in Fig. 8 (c), $Z_{0,pk}$ = 3 Ω (e.g. R_d = 1.5 Ω and C_d = 5 nF) results to be sufficient to limit $v_{ov,pk}$ below V_{dc} + 50 V and to cancel the oscillation after its first peak in the considered conditions. Correspondingly, Fig. 7 (yellow) shows how the integration of this R_dC_d network reduces $Z_{0,pk}$ from 30 Ω to 3 Ω, effectively damping the resonance. A C_b-R_dC_d network featuring a smaller $Z_{0,pk}$ (yellow in Fig. 8 (c)) does not show significant improvement on the damping performance, however, the associated value of C_d increases, complicating the integration.

Fig. 8 (b) and (d) additionally confirm how $Z_{0,pk}$ is a good indicator of the performance of the damping network. Given the shape of the isolines, Fig. 8 (d) shows three measurements where, even changing the value of C_d, $Z_{0,pk}$ remains between 4 Ω and 5 Ω. As a consequence, the resulting vov waveforms are similar in the three cases. Differently, the three measurements reported in Fig. 8 (b) cover almost the full range of $Z_{0,pk}$ (i.e. 2.5 Ω, ... 9.4 Ω) and the performance of the damping network significantly improves (i.e. from almost ineffective to comparable with the optimized design). Ultimately, the values reported in the first row of TABLE V (L_{ext} = 15 nH) are selected.

In Fig. 8 (a), the locus of [33]-optimum solutions, revisited to consider the influence of R_{ac}, is additionally marked with a white dashed line. As expected, fixed $Z_{0,pk}$ (i.e. an isoline), it selects the corresponding design featuring minimum C_d. Therefore, an alternative usage of the 2D-plot of Fig. 8 (a) consists in finding the value of R_d minimizing $Z_{0,pk}$ once the maximum value of C_d is given, e.g. from volume constraints. The entire optimization procedure is repeated for L_{ext} = 35 nH and the values of the resulting components are also reported in TABLE V for comparison. Intuitively, a bigger C_d

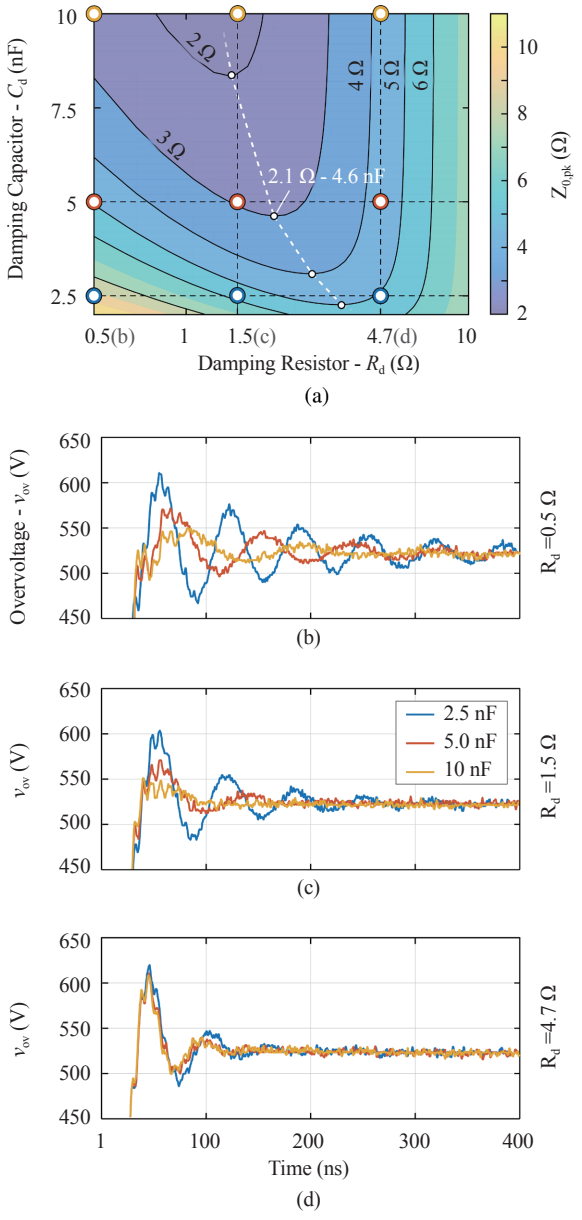

Fig. 8. Peak of the output impedance of the buffer-damping network ($Z_{0,pk}$) for 0.5 Ω < R_d < 10 Ω and 2 nF < C_d < 10 nF (a). The colored dots highlight the combinations of R_d and C_d whose associated v_{ov} measured waveforms are shown in (b), (c) and (d). Finally, the white dashed line represents the locus of the optimum designs according to [33]. C_b is fixed to 2.5 nF, L_{ext} to 15 nH and R_{ac} to 200 mΩ.

is now required to limit $Z_{0,pk}$ to 3 Ω, given the bigger L_{ext}. In order to understand the correlation between the optimized designs and the value of L_{ext}, the sensitivity of $Z_{0,pk}$ towards L_{ext} is calculated and the results are reported in Fig. 9, where the orange and light green curves are relative to the networks of TABLE V. Given the same C_b = 2.5 nF, the damping network designed for L_{ext} = 15 nH requires only half of the overall capacitance but features four times higher sensitivity compared to the design optimized for L_{ext} = 35 nH. Being $Z_{0,pk}$ the figure-of-merit of the damping network, depending on the application, the second solution could be preferred. In fact, for the first design, considering 152 $\frac{m\Omega}{nH}$ only 10 nH

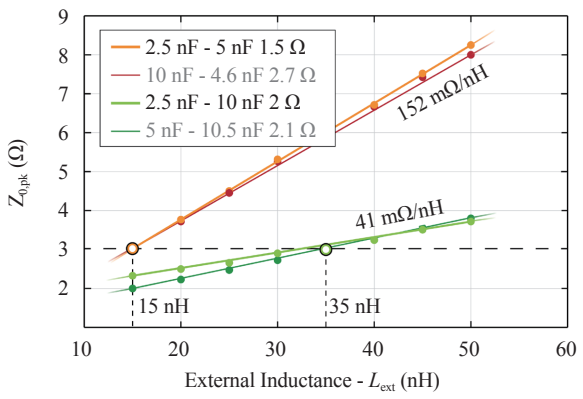

Fig. 9. Sensitivity of Z_0, representing the figure of merit of the C_b-R_dC_d network, towards L_{ext} for different [33]-optimized combinations. When the network is designed ($Z_{0,pk}$ = 3 Ω) for 15 nH (orange and red), the required overall capacitance is less than in the case of 35 nH (light and dark green), however the sensitivity is almost four times higher.

more than expected results in $Z_{0,pk}$ = 4.5 Ω and sub-optimal performance comparable to Fig. 8 (c). This information is important because Lext is typically unknown to the PM designer who is sizing the C_b-R_dC_d network. Consequently, $Z_{0,pk}$ should be set with a certain margin to the desired limit (e.g. $Z_{0,pk}$ = 1.5 Ω to obtain 3 Ω when L_{ext} is 10 nH more than expected) or a worst case L_{ext} should be considered.

The behavior of the two optimized snubbers (TABLE V) is finally examined. The measured peak voltage across R_d amounts to around 50 V in both cases and is therefore not of concern. Differently, the occurring losses could be problematic: in the considered setup, with a switching frequency of 30 kHz, the losses amount to 0.75 W and 1.25 W in the case of L_{ext} = 15 nH and 35 nH respectively. Intuitively, a more critical situation (i.e. L_{ext} = 35 nH) generates more losses to achieve the same performance. Nevertheless, in both cases a power resistor rated for 2 W (*Vishay™ Thin Film* power resistors [37]) can be used, as shown in Fig. 3.

V. Design Procedure Guideline

After clarifying the optimization of the damping network, a guideline of the described procedure for the design of the C_b-R_dC_d network (Section III and IV) is provided in this section (cf. Fig. 10). First, the followed measurements-based approach is considered:

(i) *Worst Case Conditions:* setup the DPT in the worst case scenario, i.e. for the highest V_{dc}, I_{out}, L_{ext} and L_g.

(ii) *Optimization Constraints:* define the safety margins $v_{gs,max}$ and $v_{ov,max}$. Limit the maximum value of C_b and C_d that can be integrated in the PM, e.g. a 1210 ceramic chip (C_{max}) due to limited volume.

(iii) ***Buffer Capacitor:*** measure $v_{ov,pk}$ after a hard turn-off switching transition of T_L in the DPT setup. Iteratively decrease the value of R_g and increase the value of C_b until the highest switching speed (R_g = 0 Ω or v_{gs} > $v_{gs,max}$) limiting $v_{ov,pk}$ < $v_{ov,max}$ with C_b < C_{max} is reached (cf. Fig. 6 (a)). Further increasing L_{ext} only slightly

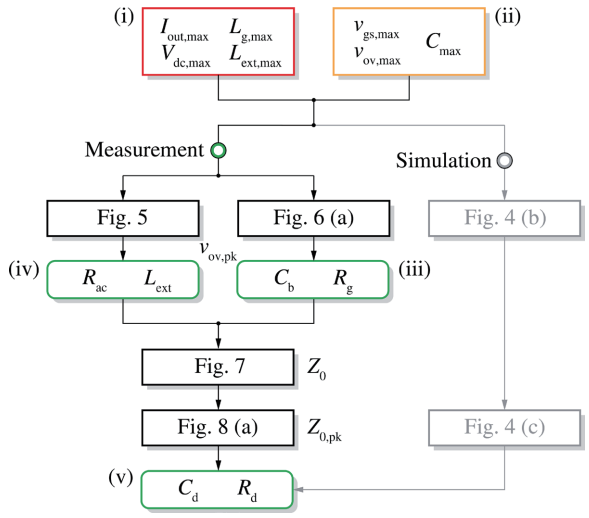

Fig. 10. Flow-chart providing a guideline for the design of the C_b-R_dC_d network as presented in this paper. Set the worst case conditions, the experiments described in Fig. 6 (a) define the required value for C_b, while the procedure presented in Fig. 8 (a) results in the optimized damping network R_dC_d. A simulation based approach, considering the equivalent circuit of Fig. 4 (c), gives accurate results once precise initial conditions and values of the parasitic elements are set.

increases $v_{ov,pk}$ (cf. Fig. 6 (b)).

(iv) *Parasitic Elements:* extract the values of L_{ext} and R_{ac} from the ringing and the damping at v_{ov} (cf. Fig. 5).

(v) ***Damping Network:*** for given C_b, L_{ext} and R_{ac} calculate Z_0 for a defined range of R_d and $C_d < C_{max}$ (cf. Fig. 7). Plot $Z_{0,pk}$ as a function of R_d and C_d (cf. Fig. 8 (a)) and select the R_dC_d pair minimizing $Z_{0,pk}$.

(vi) *Verification:* $v_{ov,pk}$ is reduced further below $v_{ov,max}$ and the oscillation is optimally damped (cf. Fig. 8 (c)). Measure the losses occurring in R_d to guarantee continuous operation. Further increasing L_{ext} only slightly worsen the damping performance (cf. Fig. 9).

If at the end of the procedure the result is too conservative, the constraints on $v_{ov,max}$ and C_{max} can be tightened and the steps from (iii) on repeated. A more compact or more efficient, but as well effective, design is obtained. Differently, if the specifications cannot be met, the mentioned constraints must be loosened or L_{ext} must be reduced.

A simplified simulation-based approach is validated in parallel to the entire analysis. The equivalent circuit shown in Fig. 4 can reproduce the damped and undamped measured waveforms of v_{ov} once all its parameters are correctly set. While the values of the parasitic elements $R_{ac}(f)$, L_{ext} and L_{CL} can be entrusted to FEM simulators, the amplitude of the current step exciting the circuit, i.e. the peak of the switched current $i_{out,pk}$ is unknown. Unfortunately, the capacitive current peak and the reverse recovery current peak, non-linear and correlated to the MOSFETs' characteristics and dynamics, add to the load current i_{out}. Therefore, either full confidence is placed on the *Spice* model of the MOSFETs (when available), or conservative assumptions, based on the MOSFETs datasheet, are necessary. Nevertheless, the analytical approach summarized in Fig. 4 (c) and TABLE IV is valuable, especially for a preliminary analysis of the problem.

Finally, it is worth noticing that the applicability of the guideline can be generally extended to PMs without integrated buffer capacitors and to PCB-based converters where C_{dc} does not find place in the closest proximity of the bridge-leg.

VI. Conclusion

A novel, ultra-low inductance (i.e. 1.6 nH) *All-SiC* PM for *More Electrical Aircraft* application featuring a planar interconnection technology is analyzed in this paper.

Despite the low parasitic inductance of the PM, the full exploitation of SiC power MOSFETs' high switching speed requires precautions concerning switching overvoltages and ringing at the switching node. Measurements proved that the integration of a buffer capacitor is generally an effective measure to minimize the drawbacks associated to the parasitic inductance of the connection to the external capacitor. However, although this solution mitigates the overvoltage, it even aggravates the oscillation, as now a resonant network is formed by the two capacitors and the inductance of the interconnection. Consequently, the integration of a R_dC_d damping network is recommended. At the expenses of only 1 W of losses and in a limited footprint, the switching overvoltage peak is significantly reduced (-80%) and the oscillation is optimally damped. Both solutions are analyzed in detail, optimized for the considered setup, verified with measurements and finally commented.

Ultimately, the designed PM is operated with a gate resistance of only 1.5 Ω (in order to minimize the switching losses) without experiencing any undesired effect due do the achieved high switching speed. This outcome validates the effectiveness of the buffer-damping network and allows the designers to explore the limit performance enabled from *All-SiC* PMs featuring planar interconnection technologies.

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New Optimal Common-Mode Modulation for Three-Phase Inverters with DC-Link Referenced Output Filter

Michael Antivachis, Dominik Bortis, Ander Avila, and Johann W. Kolar

***Abstract*—A two-level inverter followed by a DC-link referenced output filter is a promising solution for high-speed low-voltage drive systems. A limitation of this power electronics topology, however lies in the high current ripple and hence additional losses occurring within the filter inductors. This shortcoming can be addressed by means of an appropriate modulation technique. This paper details two new modulation strategies, tailored to the specific characteristics of three-phase inverters with DC-link referenced output filter, utilizing the instantaneous common-mode (CM) voltage as a degree of freedom, in order to decrease the output inductor's current ripple. It is deduced that a constant (DC) CM injection modulation (DCCMM) or an AC CM injection modulation (ACCMM) with arbitrarily large amplitude yields the best performance depending on the operating point. The CM pattern that minimizes the inductor current ripple envelope results from the combination of the two schemes and constitutes the optimal CM injection modulation (OCMM). Furthermore, the proposed modulation schemes are tested on a 300 W hardware demonstrator driving a 300 krpm custom designed motor, where a reduction of the total inverter losses of up to 11% is observed.**

***Index Terms*—DC-link referenced output filter, high-speed drives, modulation scheme, optimal CM injection.**

I. Introduction

HIGH-SPEED low-voltage (LV) drive systems spread across a wide range of applications such as turbocompressor systems, drills, medical equipment and air-conditioning units [1], [2]. Typically, a two-level pulse width modulated (PWM) inverter with high switching frequency f_s is preferred in order to provide the motor with a high quality sinusoidal current that minimizes the induced machine losses (cf. Fig. 1(a)). The insertion of an AC differential-mode (DM) interface filter between the converter and the machine further smoothes the motor terminal currents and voltages [3]. An AC-side common-mode (CM) filter suppresses the high-frequency CM voltage applied to the machine terminals and hence protects the motor insulation and bearings from overvoltage stress [4]. Moreover, the CM filter is an effective measure against conducted EMI noise, since it provides to the CM currents, induced by the switching operation of the converter, a low impedance path that confines the CM noise within the inverter stage. The DC-link referenced output filter, presented in Fig. 1(a), performs simultaneously CM and DM attenuation [5]-[7] and thus is a prominent choice for LV drive systems.

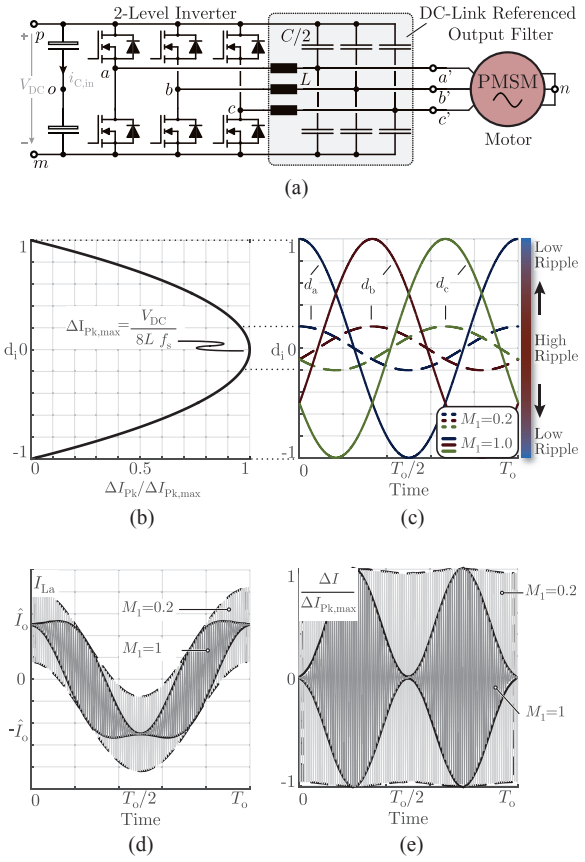

Fig. 1. In (a) the schematic of a two-level inverter with a DC-link referenced output filter followed by a high-speed motor is depicted. In (b) the correlation between the normalized peak current ripple ΔI_{Pk} and the instantaneous duty cycle d_i is presented. In (c) the sinusoidal duty cycles for two different modulation depths are shown, while in (d) and (e) the resulting inductor currents and current ripples of phase a for the different modulation depths M_1 are illustrated respectively.

Accordingly, the incorporation of a DC-link referenced output filter allows for higher motor efficiency and CM noise suppression, at the expense of decreased converter performance, since the volume and losses of the output filter are added to

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the converter stage. There has been extensive research towards counterbalancing the negative impact of the output filter by means of appropriate inverter modulation techniques [8]-[11]. For three-phase inverters employing carrier-based PWM techniques, the available degree of freedom is the shape of the injected CM duty cycle $d_{CM}(t)$ [12]. Hence, the duty cycles of the three phases can be written as

$$\begin{aligned} d_a(t) &= M_1 \cos(\omega t) + d_{CM}(t) \\ d_b(t) &= M_1 \cos(\omega t - \frac{2\pi}{3}) + d_{CM}(t) \\ d_c(t) &= M_1 \cos(\omega t + \frac{2\pi}{3}) + d_{CM}(t) \end{aligned} \tag{1}$$

where M_1 is the modulation depth defined as $M_1 = \frac{2\hat{V}_o}{V_{DC}}$ and $\hat{V}_o$ is the peak output phase voltage. Furthermore, the local average of the inverter switched voltages is given as $\langle v_{i,o} \rangle_{T_s} = d_i(t)\frac{V_{DC}}{2}$, where $i \in \{a, b, c\}$.

The aim of the CM injection with duty cycle $d_{CM}(t)$ is the minimization of the current ripple across the inductor and hence the mitigation of the inductor related losses. For example, in the case of a two-level inverter followed by an exclusive DM filter, the injection of an approximately triangular CM pattern yields the lowest filter inductor current ripple (standard space vector modulation - SVM) [13], while a sinusoidal third harmonic injection (THM) results in similarly high inductor performance. Moreover, the injection of a roughly rectangular CM component, known in the literature also as discontinuous modulation (DCM) [14], [15], leads to a reduction of the switching losses. However, in the case of a two-level inverter with a DC-link referenced output filter, the formulation mechanism of the filter inductor current i_L is fundamentally different compared to a simple DM filter, because high-frequency currents are allowed to flow through the DC-link connected capacitors $C/2$ from/towards the DC-link. Thus, the traditional modulation techniques do not yield anymore the desired performance gain. Instead, the optimal shape of injected CM duty cycle $d_{CM}(t)$, that minimizes the current ripple in the filter inductor, must be revisited and redefined according to the special characteristics of the filter topology at hand.

In response to those concerns, this paper details the degrees of freedom when selecting a modulation scheme and proposes two modulation techniques that reduce the filter inductor current ripple. In a first step, the constant CM shifting (DCCMM) of all three phases $d_{CM}(t) = M_0$ is presented, and subsequently the injection of a AC CM pattern (ACCMM) with arbitrarily large amplitude $d_{CM}(t) = -M_N \cos(N\omega t)$ (N = 3, 6, 9,...) is examined. The inductor current ripple formulation and trade-offs between the two modulation schemes are analyzed and quantified in Sec. II. Afterwards, the achievable system performance, in terms of inductor RMS current ripple, is evaluated by means of a multi-objective optimization. Based on the results, the optimal CM injection modulation scheme (OCMM) is proposed. In Sec. III, the claimed performance benefit is validated against experimental measurements and finally the conclusions are drawn in Sec. IV.

II. Generalized CM Injection Modulation

First, the current ripple formation of the filter inductor in the case of a two-level inverter with a DC-link referenced output filter is analyzed. The standard modulation case, where all duty cycles are purely sinusoidal (sinusoidal modulation - SM), i.e. without any CM pattern injection ($d_{CM}(t) = 0$), is considered (Fig. 1(c)). The switched-node voltage $v_{ao}(t)$ of phase a with respect to the DC-link midpoint o, contains a fundamental component, as well as high-frequency harmonics concentrated around and above the switching frequency f_s (cf. Fig. 2(a)). This switched voltage, with voltage levels between $+V_{DC}/2$ and $-V_{DC}/2$, is subsequently smoothed by the output filter and results in a predominantly sinusoidal terminal voltage $v_{a'n} = M_1 \cos(\omega t)$, with respect to the load open star-point n. Moreover, due to the connection of the output filter capacitors ($C/2$) to the positive and negative DC rails (p,m), a stable sinusoidal terminal voltage $v_{a'o} = M_1 \cos(\omega t)$ with respect to the DC-link midpoint o is also generated. The difference between the switch node voltage v_{ao} and the terminal voltage $v_{a'o}$ yields the current ripple inducing voltage across the inductor $v_{La} = v_{ao} - v_{a'o}$. The inductor voltage v_{La} is clearly a two-level voltage and generates an inductor current ripple similar to the case of a single-phase inverter. Due to the DC-link referenced output filter, the current ripple of each phase ΔI_{Pk} is independent of the remaining two phases (cf. Fig. 1(b)) and is determined by the duty cycle d_i(t) of the corresponding phase $i \in a, b, c$ as

$$\begin{aligned} \Delta I_{Pk} &= \frac{(1+d_i)(1-d_i)V_{DC}}{8 f_s L}, \\ \Delta I_{RMS} &= \frac{\Delta I_{Pk}}{\sqrt{3}} = \frac{(1+d_i)(1-d_i)V_{DC}}{8\sqrt{3} f_s L}, \end{aligned} \tag{2}$$

where $d_i \in [-1, 1]$.

If a triangular carrier signal is defined in the interval [−1, 1], the duty cycle that maximizes the instantaneous inductor current ripple ΔI_{Pk} is $d_i = 0$. The corresponding peak and RMS current ripple over a switching period are then calculated as

$$\begin{aligned} \Delta I_{Pk,max} &= \frac{V_{DC}}{8 f_s L} \\ \Delta I_{RMS,max} &= \frac{\Delta I_{Pk,max}}{\sqrt{3}} = \frac{V_{DC}}{8\sqrt{3} f_s L} \end{aligned} \tag{3}$$

and illustrated in Fig. 1(b).

In contrast, the current ripple is zero when the duty cycle is in the vicinity of 1 or -1. For low modulation depths M_1, the duty cycles of all three phases remain close to the zero line for the whole fundamental period T_o. As a results, the current ripple and inductor losses are maximized when the modulation depth, and hence the machine induced voltage, speed and power are low (Fig. 1(c)-(e), $M_1 = 0.2$). Conse-

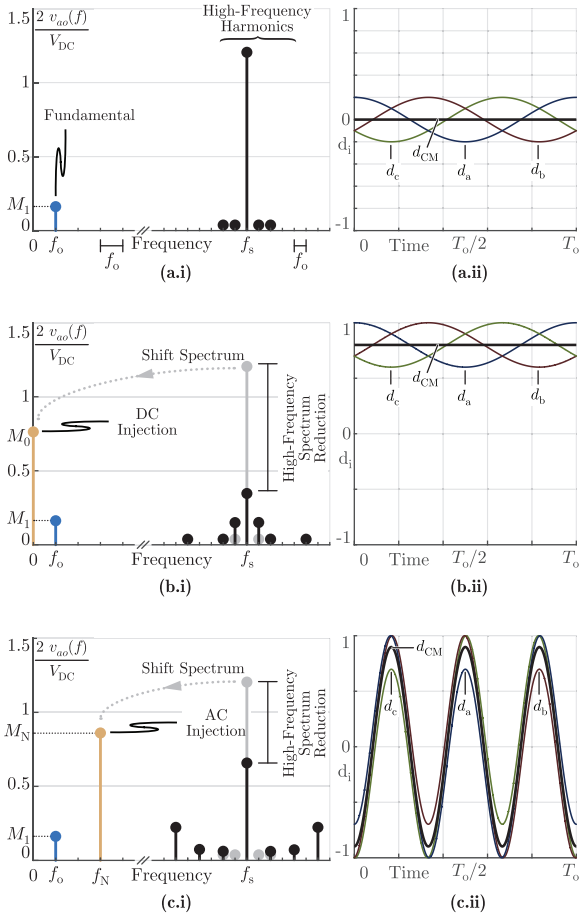

Fig. 2. In (a.i), the spectrum of the inverter switch node voltage v_{ao} is shown when the standard sinusoidal modulation (SM) of (a.ii) is employed. (b.ii) illustrates the DCCMM technique, where all the duty cycles are shifted upwards by a DC voltage component $v_{CM} = d_{CM}\frac{V_{DC}}{2}$, where $d_{CM} = M_0$. The resulting advantageous spectral shaping of the inverter voltage is depicted in (b.i), where spectral content is transferred from the switching frequency f_s to the DC component. In (c.i), the qualitative inverter voltage spectrum distribution is illustrated, when ACCMM (c.ii) modulation is employed. In this case, an AC CM component is injected to the three phase duty cycles leading to a reduction of the high frequency voltage spectrum, whereas a part of the spectral content around the switching frequency f_s is shifted to the frequency of the CM component f_N.

quently, for the standard modulation (i.e. no CM injection), the low load and part load efficiency deteriorates due to the high ratio between the losses induced within the filter inductor and the low output power. It becomes evident that steering away from the unfavorable duty cycle $d_i = 0$ is a path towards superior inductor performance. This can be achieved by means of CM injection, meaning that an identical signal $d_{CM}(t)$, either constant or variable, is added to the duty cycles of all three phases as shown in (1). This CM signal $v_{CM} = v_{no} = d_{CM}\frac{V_{DC}}{2}$ shifts the voltage of all three inverter terminal nodes either higher or lower with respect to the DC-link midpoint *o*. If examined from the frequency domain standpoint, the injection of a low-frequency CM signal advantageously shapes the spectral content of the inverter

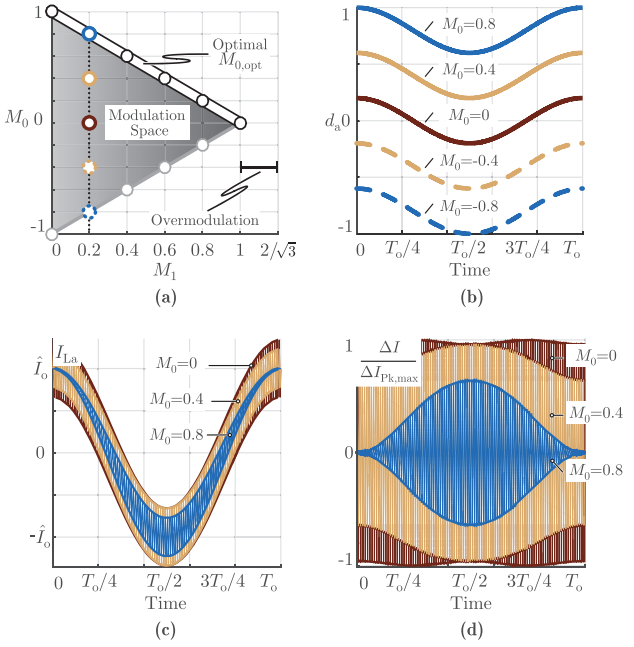

Fig. 3. Constant CM shifting (DCCMM) overview. In (a), the available M_0 values depending on the modulation depth M_1 are depicted. In (b), the effect of different values of M_0 on the duty cycle of phase *a* for a constant modulation index $M_1 = 0.2$ is visualized. In (c) and (d), the impact of the DCCMM modulation technique on the inductor current and the current ripple is shown respectively.

switch node voltage $v_{i,o}$, $i \in a, b, c$, i.e. energy is transferred from the switching frequency harmonics to the low-frequency component corresponding to the injected CM pattern (cf. Fig. 2(b.i)-(c.i)). Hence, the current ripple inducing high-frequency voltage harmonics is limited and accordingly the output filter inductor efficiency is increased. Two CM signal types are proposed and explained within the remainder of the chapter: a positive or negative constant shifting (DCCMM) (cf. Fig. 2(b.i)-(b.ii)) and an AC CM pattern (ACCMM) (cf. Fig. 2(c.i)-(c.ii)) with arbitrarily large amplitude. Both options are compared against the standard modulation scheme (SM) with purely sinusoidal duty cycles, in terms of inductor current ripple.

A. DC CM Modulation (DCCMM)

The constant CM injection strategy (DCCMM) utilizes a constant CM signal $d_{CM} = M_0$ that shifts all instantaneous sinusoidal duty cycle signals d_i away from the high current ripple region around $d_i = 0$ towards a lower ripple zone close to either $d_i = 1$ or $d_i = -1$. Hence, the CM shifting can be either positive or negative, with symmetric effects on the inductor current ripple. The constant CM shifting technique is visualized in Fig. 3(b) for the example with modulation depth $M_1 = 0.2$. For a given modulation depth M_1, the acceptable range of the M_0 injection must be defined. This can be easily derived by the constraint that all the duty cycle signals must not exceed the carrier boundaries (i.e. $-1 \le d_i \le 1$). Depending on the modulation depth M_1, the M_0 injection limits

are then calculated by

$$\begin{aligned} &M_1 \in [0,1]\ ,\ d_{\mathrm{CM}}(t) = M_0 \\ &M_0 \in [M_{0,\min}, M_{0,\max}], \\ &\text{where:} \quad M_{0,\min}(M_1) = -(1-M_1) \\ &\qquad\quad M_{0,\max}(M_1) = (1-M_1), \end{aligned} \tag{4}$$

and the available modulation space for M_0 is visualized in Fig. 3(a). It should be noted that the feasible M_0 interval becomes wider for low modulation depths M_1: for instance when $M_1 = 0.2$ (cf. Fig. 3), the M_0 parameter can be freely selected within the interval [−0.8, +0.8]. In contrast, for $M_1 = 1$, the M_0 value must be compulsively kept at zero, otherwise the instantaneous duty cycles would exceed the carrier boundaries. When $M_1 > 1$ (i.e. overmodulation), the DCCMM technique is impractical, since it provokes undesired pulse dropping which in return dramatically increases the inductor current ripple. In other words, the DCCMM scheme is only advisable for the linear modulation region, i.e. $M_1 \in [0, 1]$.

The effect of the CM injection on the current envelope is profound, which means that the current ripple envelope is contracting with increasing CM injection M_0 (cf. Fig. 3(c)), thus the CM shifting positively impacts on the inductor performance. For the simple sinusoidal modulation (SM), the current ripple reaches its maximum at the zero crossings of the duty cycle which is at the time instants $t = \frac{T_o}{4}$ and $\frac{3T_o}{4}$ (cf. Fig. 3(d), $M_0 = 0$). However, if a constant CM shifting is applied, the time instances of the zero crossing are changing. This means that for $0 < M_0 < M_1$ the two zero crossings are approaching $t = \frac{T_o}{2}$, while for $0 < M_1 < M_0$ no zero crossings take place and the maximum current ripple is solely found at $t = \frac{T_o}{2}$ (cf. Fig. 3(d) for $M_0 = 0.4$ or $M_0 = 0.8$).

B. AC CM Modulation (ACCMM)

In a second step, an alternative CM injection technique is examined which employs a sinusoidal AC CM pattern $d_{\mathrm{CM}}(t) = -M_{\mathrm{N}} \cos(2\pi f_{\mathrm{N}} t)$ with a frequency $f_{\mathrm{CM}} = f_{\mathrm{N}} = Nf_{\mathrm{o}}$ and an amplitude M_{N}. By choosing a large amplitude M_{N}, the high-frequency spectrum of the switch node voltage $v_{\mathrm{i,o}}$ is reduced and instead more spectral content is concentrated at the CM signal frequency f_{N} (cf. Fig. 2(c)). Hence, the high-frequency current ripple is reduced and superior performance in terms of losses can be achieved. Special attention should be paid to the reactive phase current flowing through the filter capacitors, since the N^{th} order harmonic current $\hat{I}_{\mathrm{C,N}}$, calculated as

$$\hat{I}_{\mathrm{C,N}} = M_{\mathrm{N}} V_{\mathrm{DC}} \pi N f_{\mathrm{o}} C, \tag{5}$$

is proportional to the amplitude M_{N} and the frequency f_{N} of the AC harmonic voltage. Especially for high speed motor drives, where the fundamental frequency f_{o} can be in the kHz-range, the reactive currents at the frequency $f_{\mathrm{N}} = \mathrm{N} \cdot f_{\mathrm{o}}$ become significant and hence should be limited. Otherwise additional conduction losses are occurring in the inductors and semiconductor devices, degrading the overall system performance. In the course of this research, which focuses on ultra-high speed drive systems, the frequency of the AC CM signal must be set to the lowest possible CM frequency $f_{\mathrm{CM}} = 3f_{\mathrm{o}}$, thus the ACCMM reduces to a generalized third harmonic modulation scheme (GTHM). According to the conventional third harmonic injection (THM), the amplitude of the third harmonic, M_3, is typically set to $\frac{M_1}{6}$ or $\frac{M_1}{4}$ in order to allow linear overmodulation (i.e. $M_1 \in [1, \frac{2}{\sqrt{3}}]$). In contrast, for the proposed generalized third harmonic modulation scheme (GTHM), the amplitude of the third harmonic M_3 is considered as a degree of freedom that can be set arbitrarily. The GTHM clearly constitutes an extension of the conventional third harmonic modulation, thus both are applicable in the overmodulation region (i.e. $M_1 \in [1, \frac{2}{\sqrt{3}}]$).

Depending on the modulation depth M_1, the maximum and minimum allowable value of third harmonic injection M_3 must be defined in a similar fashion as in the case of DCCMM, i.e. the modulation index is constrained within $-1 \leq d_{\mathrm{i}} \leq 1$. The closed form solution can be found as

$$\begin{aligned} &M_1 \in \left[0, \frac{2}{\sqrt{3}}\right]\ ,\ d_{\mathrm{CM}}(t) = -M_3 \cos(3\omega t) \\ &M_3 \in [M_{3,\min}, M_{3,\max}] \\ &\text{where: } M_{3,\min}(M_1) = -(1-M_1) \\ &M_{3,\max}(M_1) : \begin{cases} \text{Solving nonlinear equation} \\ M_1 \cos(\phi) - M_{3,\max} \cos(3\phi) = 1 \\ \phi = \sin^{-1}\left(\sqrt{\dfrac{9M_{3,\max} - M_1}{12 M_{3,\max}}}\right) \end{cases}. \end{aligned} \tag{6}$$

The corresponding modulation area, which is asymmetric, is depicted in Fig. 4(a). In Fig. 4(b), third harmonic patterns with different amplitudes are superimposed on the sinusoidal duty cycle of phase *a*, for the example of modulation depth $M_1 = 0.2$. As can be noticed, the generalized third harmonic injection shapes the current ripple envelope in a way that it is continuously alternating between high and low current ripple (cf. Fig. 4(c)) whereas the inductor current stress decreases, with increasing M_3 values (cf. Fig. 4(d)). In analogy to DCCMM, it should be noted that for GTHM the available range of M_3 values is wide for low modulation depths M_1, and for high modulation depths the M_3 parameter is increasingly restricted.

C. Optimal CM Modulation (OCMM)

The idea behind the two modulation schemes, constant CM shifting (DCCMM) and generalized third harmonic injection (GTHM) is now established. The corresponding parameters M_0 and M_3 constitute degrees of freedom and must be selected in a way that minimizes the inductor current stress. From a numerical optimization standpoint, the mod-

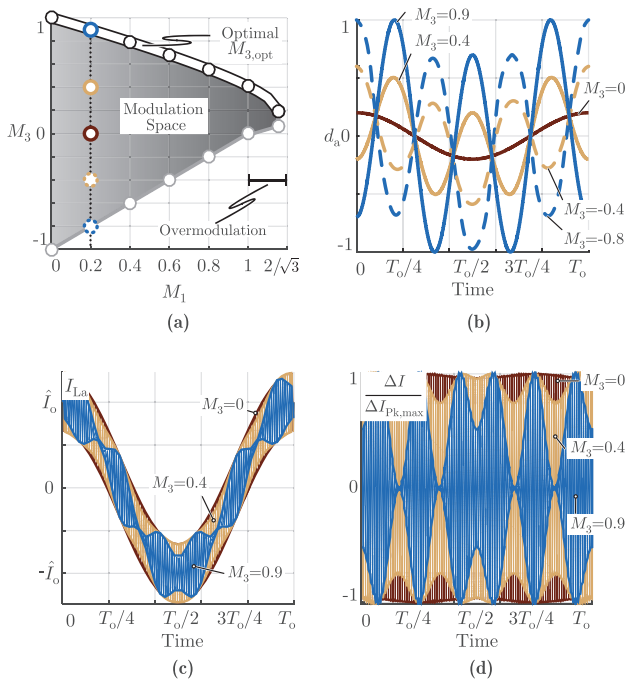

Fig. 4. Generalized third harmonic injection (GTHM) overview. In (a), the allowable M_3 values depending on the modulation depth M_1 are depicted. In (b), the effect of different values of M_3 on the duty cycle of phase *a* for a constant modulation index $M_1 = 0.2$ is visualized. In (c) and (d), the impact of the GTHM modulation technique on the inductor current and the current ripple is shown respectively.

ulation parameters M_0 and M_3, which are subject to linear constraints $M_{0,min} < M_0 < M_{0,max}$ and $M_{3,min} < M_3 < M_{3,max}$, represent the optimization variables and have to be optimized in such a way that for a given modulation depth M_1 the optimal CM values $M_{0,opt}$ and $M_{3,opt}$, resulting in the lowest inductor RMS current ripple, are found. Accordingly, the objective function F is defined as the normalized inductor RMS current ripple over a fundamental period T_o and quantifies the effectiveness of the employed parameter combination of M_0 and M_3,

$$F = \frac{\Delta I_{RMS}}{\Delta I_{RMS,max}} = \frac{\sqrt{\frac{1}{T_o}\int_0^{T_o} \Delta I_{L,a}^2(t)dt}}{\frac{V_{DC}}{8\sqrt{3}f_s L}}. \quad (7)$$

The goal of the optimization algorithm is to identify the optimal set of parameters M_0, and M_3, such that the objective function F is minimized.

The optimization procedure for the parameter M_0 of the constant CM injection techniques is analyzed first. For one modulation depth M_1 (cf. Fig. 3(b) with e.g. $M_1 = 0.2$), the acceptable M_0 parameter values (in this case $M_0 \in [-0.8, +0.8]$) are swept and for each M_0 case the resulting normalized RMS current ripple $F(M_1, M_0)$ is calculated. Subsequently, the M_0 value that results in the minimization of the objective function (i.e. minimum current ripple) is selected as optimal modulation choice $M_{0,opt}(M_1)$ (cf. Fig. 3(c),(d), $M_{0,opt}(0.2) = 0.8$). The process is iterated for all the modulation depths $M_1 \in [0, 1]$ as visualized in Fig. 5(a), and thereby the optimal value of the constant CM shifting scheme (DCCMM) is derived. It should be noted that the constant CM injection scheme is symmetric in the sense that identical performance is attained by shifting upwards by $+M_0$ or downwards by $-M_0$, while the optimization reveals that the largest $|M_0|$ leads to the lowest inductor current ripple. The optimal values of $M_{0,opt}$ depending on the modulation depth M_1 are highlighted in Fig. 3(a), while Fig. 5(c) shows how the current ripple for the optimized DCCMM technique in comparison to the standard sinusoidal modulation (SM) evolves over different operating points.

The same optimization procedure used for M_0 can be applied for the optimization of the parameter M_3 of the GTHM modulation scheme. The optimal amplitude $M_{3,opt}$ of the third harmonic that yields the lowest current ripple (i.e. minimizes $F(M_1, M_3)$) is calculated for each modulation index M_1 and thus the optimal third harmonic injection modulation scheme is derived (cf. Fig. 5(b)). In this case, the inductor current ripple changes in an asymmetric fashion with respect to M_3. Indeed, the amplitudes of the third harmonic $+M_3$ and $-M_3$ (negative amplitude indicates phase shift of 180°) result in different inductor performance. In analogy to the DCCMM, the optimization deduces that the maximum positive amplitude of third harmonic always yields the best inductor performance as visualized in Fig. 4(a). A key feature of the GTHM is that in contrast to the DCCMM it can also be used in the over modulation region $M_1 \in [1, \frac{2}{\sqrt{3}}]$. The minimum current ripple achievable by employing GTHM over the whole converter operation range is plotted in Fig. 5(c), and is compared against the corresponding performance of the sinusoidal modulation (SM).

A possible combination of two CM injection patterns (DCCMM, GTHM) is also investigated. In this case, the inserted CM pattern is $d_{CM} = M_0 - M_3 \cos(3\omega t)$. The results reveal that merging both modulations (i.e. simultaneously $M_0 \neq 0$ and $M_3 \neq 0$) does not yield superior performance in terms of current ripple. Instead for low modulation indexes $M_1 < 0.5$ the exclusive utilization of constant CM shifting (DCCMM) (i.e. $M_0 \neq 0$, $M_3 = 0$) allows for the smallest current ripple, while for high duty cycles $M_1 > 0.5$ the generalized third harmonic injections (GTHM) is more effective (i.e. $M_0 = 0$, $M_3 \neq 0$). The modulation scheme that transitions from DCCMM (below $M_1 = 0.5$) to GTHM (above $M_1 = 0.5$) constitutes the optimal CM injection modulation (OCMM) as indicated in (Fig. 5(c)) and minimizes the inductor losses over the whole inverter operating range. At the transition point $M_1 = 0.5$, the parameter M_0 must be decreased while the parameter M_3 must be increased in a way such that all the duty cycles remain within the carrier limits, and that the output DC-link referenced filter is not excited. To this end a smooth transition is proposed according to which the values of M_0 and M_3 are progressively adjusted within a transition interval $M_1 \in [0.4, 0.6]$ around the transition point $M_1 = 0.5$. Namely, the parameter M_0 is linearly decreased with respect to M_1, from $M_0 = 0.6$ at $M_1 = 0.4$ to $M_0 = 0$ at $M_1 = 0.6$. Accordingly the parameter M_3 is increased from $M_3 = 0$ at $M_1 = 0.4$ to $M_3 =$

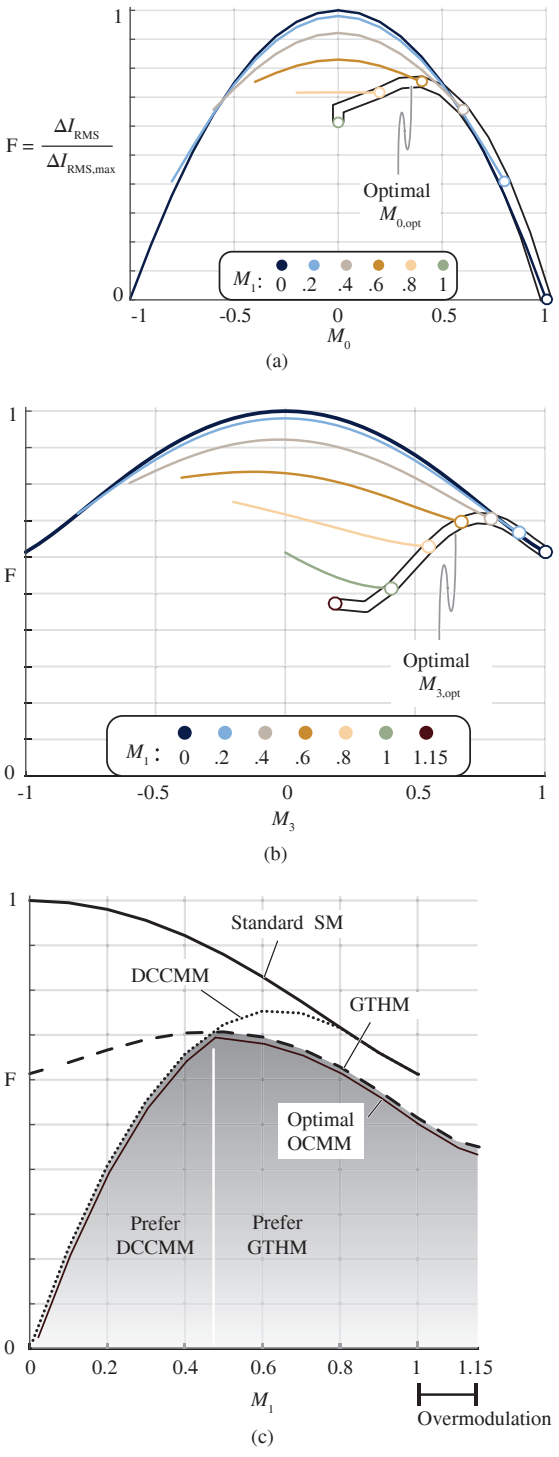

Fig. 5. Optimization procedure of the DCCMM and GTHM modulation parameters M_0 and M_3. In (a), the DCCMM strategy is analyzed: for each modulation depth M_1 all the possible values of the optimization parameter M_0 are sweped and the corresponding normalized current ripple is calculated for each value. The $M_{0,opt}$ value that yields the lowest RMS inductor current ripple F (cf. (7)) constitutes the optimal choice and is highlighted. In (b), the same optimization method is visualized for the case of GTHM and the parameter value M_3. The optimal set of parameters $M_{0,opt}$ and $M_{3,opt}$ for each modulation depth M_1 are visualized in Fig. 3(a) and Fig. 4(a) respectively. Finally, in (c), the performance of the optimized DCCMM and GTHM, in terms of current ripple, is depicted and is compared against the standard sinusoidal modulation (SM).

0.68 at $M_1 = 0.6$. The proposed transition strategy ensures uninterrupted inverter operation at the expense of increased current ripple (suboptimal selection of M_0, M_3 in the transition region).

D. Inverter Component Stress

In order to provide a comprehensive overview of the total inverter performance when the OCMM is employed, the stresses on the remaining converter components (i.e. DC-link capacitor, power semiconductors) are derived by means of analytic closed form expressions. There, a sinusoidal output inverter current $I_{L,a} = \hat{I}_o \cos(\omega_o t - \Phi)$ (i.e. current ripple is neglected), slightly lagging the motor AC voltage $v_{a'n} = M_1 \frac{V_{DC}}{2} \cos(\omega_o t)$ by the phase angle Φ (i.e. low reactive power consumption), is assumed in the course of the calculations [16].

For the stress analysis of the power semiconductors, first the RMS current stress of the top- and low-side devices of phaseleg a are examined. The same consideration can be extended to the remaining two phases due to symmetry. The local RMS current (i.e. over one switching period T_s) of the low and high side switches of phase-leg a are calculated as follows,

$$\begin{aligned} \langle I_{a,High,RMS}(t) \rangle &= \sqrt{\frac{1+d_a(t)}{2}} \cdot I_{La}(t), \\ \langle I_{a,Low,RMS}(t) \rangle &= \sqrt{\frac{1-d_a(t)}{2}} \cdot I_{La}(t), \end{aligned} \tag{8}$$

where $d_a(t) = M_1 \cos(\omega t) + M_0 - M_3 \cos(3\omega t)$.
Based on the local RMS values, the global RMS current stress over a fundamental period T_o can be calculated as

$$\begin{aligned} I_{a,High,RMS} &= \sqrt{\frac{1}{T_o}\int_0^{T_o} \langle I_{a,High,RMS}(t) \rangle^2 \, dt} = \hat{I}_o \sqrt{\frac{1+M_0}{4}}, \\ I_{a,Low,RMS} &= \sqrt{\frac{1}{T_o}\int_0^{T_o} \langle I_{a,Low,RMS}(t) \rangle^2 \, dt} = \hat{I}_o \sqrt{\frac{1-M_0}{4}}. \end{aligned} \tag{9}$$

As can be noted from (9), in the case of DCCMM (i.e. $M_0 \neq 0$, $M_3 = 0$), the RMS current burden is unequal between the top- and low-side switch. For example, when positive DC CM shifting ($M_0 > 0$) is selected, the duty cycles of all three phases are shifted upwards and therefore the relative on-time of the high-side semiconductors is longer than the corresponding on-time of the low-side devices. Hence, higher RMS current stress and losses on the high-side switches are caused (9). For increasing M_0 values, which are only present for low modulation depths M_1, the unequal current sharing becomes more pronounced. In this case, however, in many motor drive applications (e.g. compressors) the speed, the EMF and the current amplitude $\hat{I}_o$ of the motor are small and accordingly the unequal distribution of the current stress on both high and low devices is no more critical. On the contrary, the GTHM (i.e. $M_1 = 0$, $M_3 \neq 0$) modulation equally distributes the current stress among the semiconduc-

TABLE I
HARDWARE DEMONSTRATOR SPECIFICATIONS

Parameter	Value
Motor	
Speed n	300 krpm
Resistance R_{m}	0.041 Ω
Inductance L_{m}	4.72 µH
Power P	300 W
Losses $P_{\mathrm{Loss,m}}$	5 W
Inverter	
DC-link voltage V_{DC}	48 V
Output phase RMS voltage $\tilde{V}_{\mathrm{o}}$	19 V
Fundamental frequency f_{o}	5 kHz
Switching frequency f_{s}	140 kHz
Filter inductance L	17 µH
Filter capacitance C	1.33 µF
Power density ρ	1.91 kW/dm^3
Efficiency η	97.29% (≈ 9 W losses)

tors, since the expressions of (9) do not depend on M_3. The switching performance remains roughly unaffected from the employed modulation scheme, since the same total number of switching transitions occurs independent of the modulation strategy.

The input DC-link capacitor conducts the high frequency switched current $I_{\mathrm{C,in}}$, which in return causes losses in the equivalent series resistance (ESR), and could reduce the life time especially for aluminium electrolytic capacitors. A simple expression relating the capacitor RMS current with the modulation depth M_1 and the AC-side power factor cos(Φ) is given in [17], which is independent of the applied inverter control scheme,

$$I_{\mathrm{C,in,RMS}} = \frac{\hat{I}_{\mathrm{o}}}{\sqrt{2}}\sqrt{2M_1\left[\frac{\sqrt{3}}{4\pi}+\cos^2(\phi)\left(\frac{\sqrt{3}}{\pi}-\frac{9}{16}M_1\right)\right]}. \quad (10)$$

This analytic approximation assumes sinusoidal inverter output currents and thus neglects the marginal increase of the input capacitor current stress caused by the output current ripple (up to 8% - [17]). Large circulating CM currents, flowing through the DC-link referenced output filter capacitors $C/2$ in the case of GTHM ((5) - $\hat{I}_{\mathrm{C,3}} = M_3 V_{\mathrm{DC}} \pi 3 f_{\mathrm{o}} C$), could further increase the input capacitor RMS current. However, the small capacitance values $C/2$ typically selected for the implementation of the output filter in order to minimize the fundamental reactive phase current $\hat{I}_{\mathrm{C,1}} = M_1 V_{\mathrm{DC}} \pi f_{\mathrm{o}} C \leq 0.1\, \hat{I}_{\mathrm{o}}$, inherently limits the CM currents $\hat{I}_{\mathrm{C,3}}$. Therefore, the effect of the small circulating CM currents can also be disregarded and the analytic expression (10) can be used for the DC-link capacitor design and loss estimation when any of the discussed modulation schemes SM, DCCMM, GTHM or OCMM is employed.

III. EXPERIMENTAL VALIDATION

In order to validate the claimed performance benefits derived from the proposed CM injection techniques, a hardware demonstrator was assembled and tested. Thereby, an industry solution example of a high-speed motor drive, which features an output power of 300 W and a rotational motor speed of 300 krpm, is used. The detailed specifications are recapitulated in TABLE I, while the test setup is visualized in Fig. 6(a). The hardware prototype includes a two-level inverter employing the latest generation of GaN devices and a DC-link referenced output filter as depicted in Fig. 6(b). A two-pole permanentmagnet (PM) slotless design, able to withstand the mechanical stress related to the high rotational speeds and exhibiting very low leakage inductance [18], [19], is selected for the high speed machine implementation. The custom 300 krpm motor prototype (cf. Fig. 6(c)) is built in a back-to-back (B2B) configuration. In particular, the inverter driven motor is connected to the same shaft as an identical generator, which subsequently feeds a diode rectifier with an adjustable DC load (cf. Fig. 6(a)). Thereby, the torque and the speed of the motor can be adjusted independently, offering maximum testing flexibility. A cascaded speed and current controller in dq-axis reference frame is implemented using a digital signal processor (DSP) in order to drive the machine. The motor angle ϵ is provided by a hall sensor board

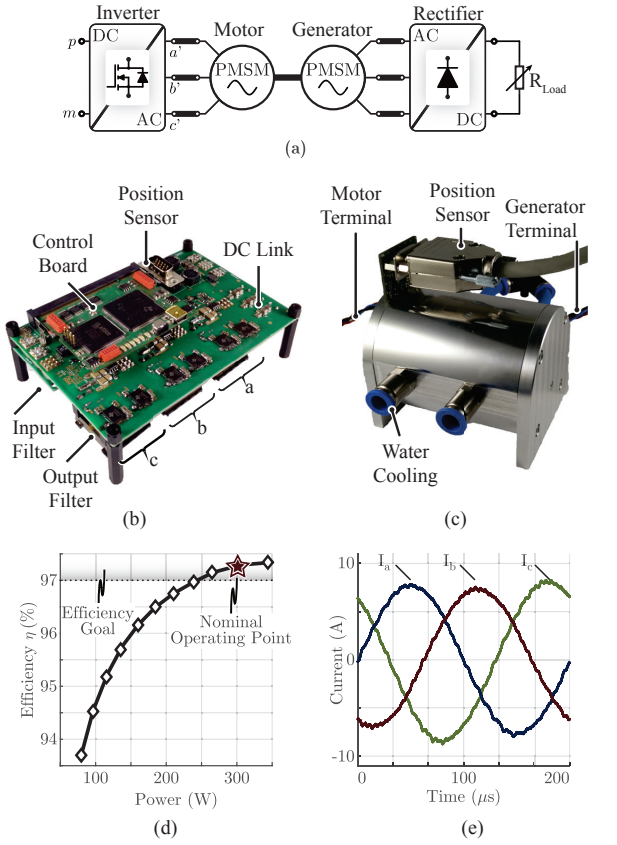

Fig. 6. An overview of the high-speed motor drive test setup employed for the experimental verification is depicted in (a). In (b), the two-level inverter prototype with a DC-link referenced output filter is shown, while in (c), the constructed ultra-high speed permanent-magnet motor is presented. In (d) the inverter efficiency curve is plotted over the whole power range when sinusoidal modulation (SM) is utilized. In (e), the measured smooth sinusoidal motor currents under nominal speed (i.e. 300 krpm) and power operation are shown. The slight imbalance of the phase currents originates from asymmetric geometric construction of the phase windings.

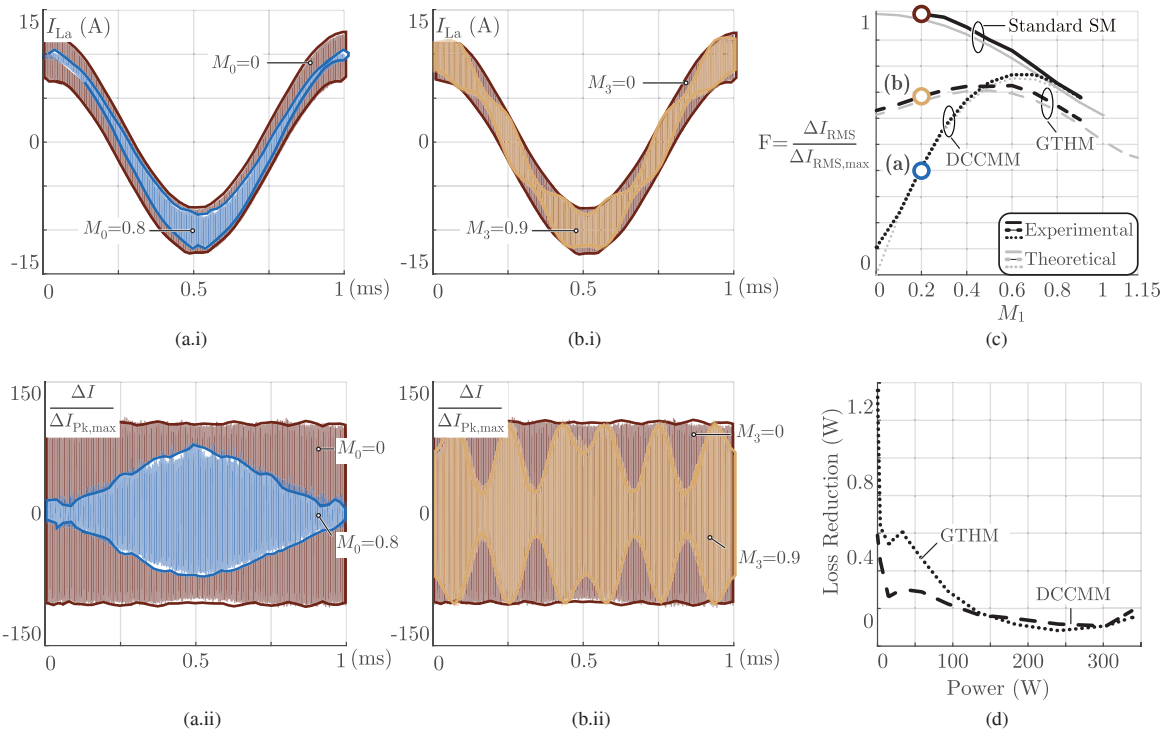

Fig. 7. In (a.i), the measured inductor currents with (M_0 = 0.8) and without (M_0 = 0) DCCMM are depicted. The fundamental frequency is f_s = 1 kHz and the modulation depth is M_1 = 0.2. Afterwards, the inductor current ripple is derived by means of data post-processing in (a.ii). The same quantities are plotted in (b.i) and (b.ii) for the same modulation depth M_1 = 0.2 when GTHM is employed. In (c), the measured inductor current ripple ΔI_{RMS} is compared with its theoretically calculated counterpart (cf. Fig. 5(c)). In (d), the reduction of the losses attained by the two proposed modulation techniques (i.e. DCCMM and GTHM), compared to the standard sinusoidal modulation (SM), is plotted.

that is directly mounted on the machine chassis. Standard sinusoidal modulation (SM) is initially employed in order to commission the inverter-motor combination. The measured inverter efficiency curve and the nominal motor currents at a rotational speed of 300 krpm are shown in Fig. 6(d) and (e) respectively.

In a next step, the two proposed modulation schemes are implemented. The optimal values of the CM injection parameters $M_{0,opt}$ and $M_{3,opt}$ corresponding to different modulation depths M_1 (cf. Fig. 3(a) and Fig. 4(a)) are stored in a lookup table (LUT) within the microcontroller memory and are accessed seamlessly during system operation. Depending on the applied modulation depth M_1, the optimal injection parameter is directly selected from the LUT or a linear interpolation between the two nearest values is performed. For a motor speed of 60 krpm (i.e. fundamental frequency f_s = 1 kHz) and the rated motor torque (i.e. rated motor current 10 A, M_1 = 0.2), the two proposed methods, DCCMM and GTHM, were tested and the measurement results are plotted in Fig. 7(a),(b). The beneficial shaping of the inductor current ripple envelope is evident for both modulation strategies. Based on the experimental measurements, the RMS inductor current ripple ΔI_{RMS} is extracted for different operating points and is compared against the theoretically calculated values. An excellent matching between the theoretical and experimental results is observed in Fig. 7(c). Finally, the inverter losses are measured for multiple power levels $P \in$ [0 W, 350 W]. The achieved loss reduction by employing DCCMM or GTHM, compared to the standard sinusoidal modulation (SM), is shown in Fig. 7(d). The loss reduction is originating exclusively from the minimization of the inductor current ripple. Especially for low modulation depths, where a wider range of CM injection parameters M_0 and M_3 is available (cf. Fig. 3(a) and Fig. 4(a)), the loss benefit is more significant. At the best case, a reduction of the converter losses by $\simeq$ 1 W with respect to the nominal converter losses of 9 W is exhibited.

IV. Conclusions

Two new modulation techniques, towards highly efficient low-voltage inverters are proposed and analyzed in this paper. The need for new modulation schemes, beyond the state-of-theart solutions, is established for the case of a two-level inverter followed by a DC-link referenced output filter. The degree of freedom, when selecting a modulation technique, is the injected CM voltage pattern $d_{CM}(t)$. The unique inductor current ripple formation of the DC-link referenced filter motivates the reconsideration of the optimal CM injection waveforms. The proposed constant CM shifting of the duty cycles (DCCMM) is described first, and afterwards the generalized third harmonic injection modulation (GTHM) is introduced. The main idea behind both schemes lies in the shifting of the inverter switched voltage spectral content

from the switching frequency towards a low CM modulation frequency (i.e. $f_{CM} = 0$ or $3f_o$). Both methods are evaluated by means of optimization in terms of inductor current ripple. It is concluded that for low modulation depths the DCCMM is more effective, while for high modulation indexes the GTHM yields superior performance. Finally, a benchmark high-speed motor drive is assembled, including a 300 W converter and 300 krpm motor. The hardware demonstrator is successfully used as framework in order to validate the functionality and effectiveness of the proposed modulations schemes. A loss reduction up to 11% is attained compared to standard sinusoidal modulation.

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